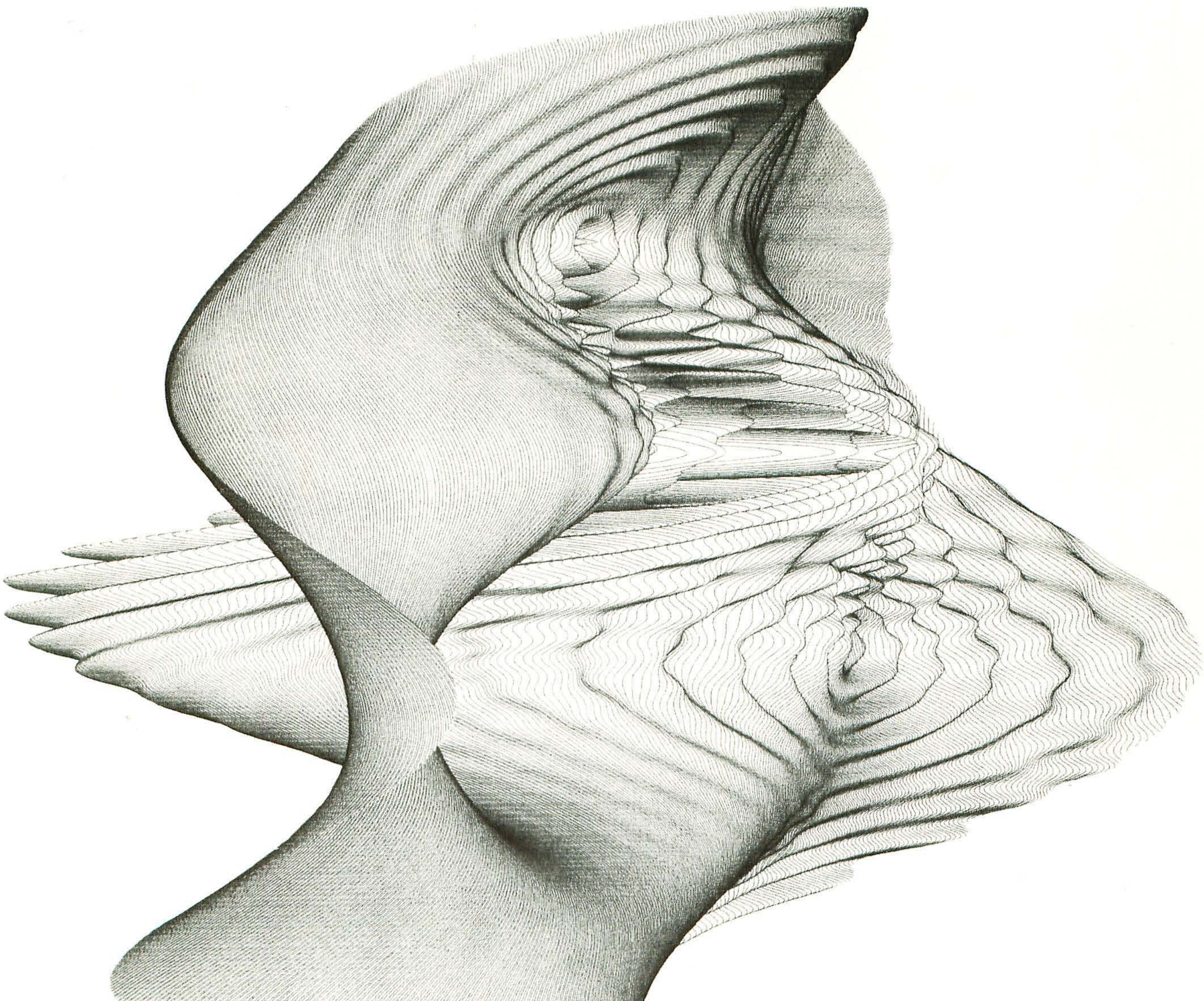
FEBRUARY 1977 VOLUME 2, Number 2 $1.50

BYTE

the small systems journal



SwTPC NEWS

More Memory-Same Price
4K Now Standard In 6800

San Antonio–The SwTPC 6800 computer system, always a best buy is now an even greater bargain. Price reductions by the manufacturers of MOS memory circuits have made it possible to now offer the standard $395.00 6800 computer kit with 4K of memory instead of 2K as previously. Memory circuits are 21L02 types which make possible powering up to 24K of memory in the stock chassis with the standard power supply.

The Southwest Technical 6800 at $395.00 includes everything needed to work with your terminal. You get 4K of static MOS memory and a serial interface as part of the basic package. These are not extra cost options (?) as in many computer systems on the market.

8K MEMORY CARDS ANNOUNCED –

For those 6800 systems needing the maximum possible amount of memory, Southwest Technical Products announces 8K memory cards. These memory expansion cards have 8K Bytes of low power MOS memory per board. These kits feature the new 4K static RAMS that are now becoming available. These new RAMS make it possible to put 8K of memory on a board without crowding the parts, or using small hard to solder connecting lines. These new memory boards feature DIP switch address selection and a write protect switch on each board.

The low power consumption of this new memory board makes it possible to use up to 48K of memory in the standard 6800 chassis with the stock power supply. Priced at $250.00 these memory cards cost no more than less dense memories from other sources.

PRICES CUT ON 4K MEMORIES

Southwest Technical Products has reduced the price of its standard 4K memory card by 20%. These cards use low power 21L02 static memories. The new price for the MP-M memory kit is $100.00 for a full 4K kit.

This kit contains 4K of memory with full buffering and dual on-board voltage regulators. Six of these memory cards may be used in a standard 6800 chassis to provide 24K of memory for the system. Memory now becomes even more of a bargain–24K for only $600.00.

Who Needs It?

We continue to get reports from customers who are amazed at the ease of assembly of the 6800 computer. One reports that he purchased test equipment before ordering a computer at the advice of friends who owned brand "X" machines. His total use of the test equipment was zero (0) when he installed each board in the 6800 and they all proceeded to work perfectly the first time. He later found in comparing notes with other 6800 owners that his was not a unique experience.

People who have built most of the various types of computers on the market generally agree that our instructions are the best and most complete. So don't worry about purchasing the least expensive computer system, there are still good honest values being offered in the world of personal computing.

SUPER SOFTWARE

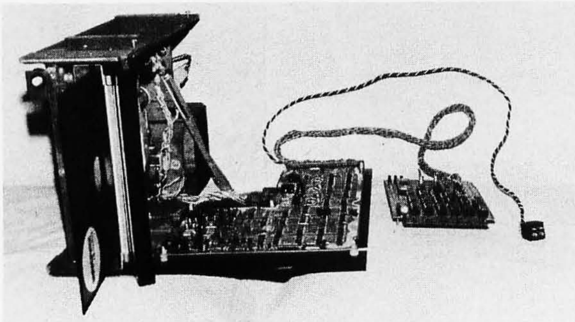
"Lack of Software" can no longer be used as an excuse by those who have the poor taste to purchase computers using older, less elegant processors than the MC-6800. Southwest Technical Products has not only editor-assembler and game programs available for the 6800, but also both 4K and 8K BASIC.

The ability to run ANSII standard BASIC programs on the 6800 make the enormous number of BASIC programs out there all usable on the SwTPC 6800. That's right, you can run anyones BASIC programs on the 6800 provided they are written in standard BASIC (as most are). 4K Basic at $4.95 and 8K BASIC at $9.95 are inexpensive enough for anyone to own. They do not cost hundreds of dollars as in some systems, or only become available when combined with purchase of huge amounts of memory as in others.

Loading even a relatively long program such as 8K BASIC into your SwTPC 6800 is not a long procedure when the AC-30 cassette interface is used. This super reliable and inexpensive ($79.95 complete with cabinet and power supply) cassette interface uses the "Kansas City" standard format and will load 8K BASIC in approximately five minutes.

SOUTHWEST TECHNICAL PRODUCTS CORPORATION
219 W. Rhapsody
San Antonio, Texas 78216

In This BYTE



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The computer was created to free mankind from the drudgery of doing tiresome chores best left to an automaton. In most computers, there is an extremely helpful monitor program such as the SYS 8 program available in versions by IMSAI and Processor Technology. Sometimes, the writers of such programs leave the user with a few residual chores to do, like entering line numbers for each command or operation. Bill Nico wasn't satisfied with that, and proceeded to patch in an automatic line numbering feature for SYS 8, described in his article on **Sweet Auto Line**.

A key component of a usable system concept is the mass storage subsystem. In this issue, Jack Breimeir, one of the engineers on the Phi-Deck design, and Ira Rampil of the University of Wisconsin begin a two part article on **The Digital Cassette Subsystem.** In part 1 you'll find some background information on digital recording, and details of the problem of head interface electronics for digital recording.

Mass storage is the critically important component of a personal computing system which is often passed up on grounds of price or complexity. People tend to have preconceived ideas that a controller which is a complicated technological nightmare will double the price of a drive alone. However, demonstrations of accomplishment are a way to dispel preconceived biases. Dr Kenneth B Welles shows in his article on the **Economy Floppy Interface** that buying just a couple of drives and building a relatively inexpensive homebrew controller can give anyone the advantages of over 200 K bytes on line per drive. His circuit takes just 17 common integrated circuits (one of which is an LSI communications processing device).

Color television interfaces are starting to become popular. However, not everyone has a color television sitting around idly. Is it possible to have a color terminal and not have to use a color television set? Subjective color is a possibility that is explored by Steve Bain in his article **Color Displays on Black and White Television Sets.** Read Steve's article and find out how you too may be able to add a color modulation effect to a black and white television set.

Serial storage media are widely used in low cost computer systems. They range in performance from paper tape through cassette tapes with manual controls to high performance programmably controlled cassettes, tape cartridge drives and full industry standard magnetic tape drives. Find out some of the background information pertinent to use of most magnetic tape serial media in Brian D Murphy's article, **Serial Storage Media: An Introduction and Glossary.**

Human interactions with computers go both ways. For computer outputs, most people think in terms of visual displays. This completely ignores the use of other senses like hearing (or touch or smell for that matter). In **Audible Interrupts for Humans,** Charles F Douds describes a simple circuit which can take advantage of the audio channel of the human system.

Here you are, a novice or experienced flier, cruising along in your ancient Cub under VFR conditions when ... all of a sudden, VFR becomes IFR and you can't see. If you had an inexpensive Omega navigation system in a portable package in your copilot's seat, you'd at least know where you are on the map with an accuracy of about 1 mile. In his article **Cub 54, Where Are You? (Or How to Navigate Using Mini-O)**, Ralph Burhans begins a multiple article discussion on Omega navigation, design of an Omega receiver for use with a small computer as a personal navigation system, and software for determination of position information. Aviation enthusiasts and boating enthusiasts who are into microcomputers will be able to use this information to help make an experimental robot navigator.

Is it an impossible dream? Is it conceivable to make an audio cassette IO port with only a single bit line in each direction? Well, if you ignore the need for connecting wires, clipping diodes and isolation capacitors, then you can use a "hardwareless" software technique such as that described in Daniel Lomax's **The Impossible Dream Cassette Interface.**

Most of today's microprocessors have all of their functions centralized without a single device. The F8 microprocessor by Fairchild Semiconductor is unique in that it divides the system functions among several basic circuits. In his article, **Microprocessor Update: The F8 System**, Robert Baker describes this rather unique way of approaching the development of a microprocessor system.

Upon receiving that first microprocessor, the budding computer hobbyist is often confronted with disdainful stares and must endure such comments as, "Well now, let's see it do something." If you have a Motorola 6800 based system with MIKBUG, John Rathkey's article, **A MIKBUG Roadmap . . .**, will aid you in getting your system to "do something" that will satisfy even the most doubting of your critics.

In several manufactured products which have been appearing lately, a hexadecimal input keyboard is one feature of the computer processor. Joseph Hoegerl describes how this sort of **Calculator Keyboard Input for the Microcomputer** can be wired up and used to replace toggle switches. His version is for an 8008 system, but the same hardware is applicable to other computers as well.

If you are interested in designing your own TTL circuits you should be aware that there is a definite limit to the number of gates that can be interconnected. In **TTL Loading Considerations** Greg Tomalesky explains how these limits are determined by circuit designers and gives advice on what pitfalls to watch out for when designing your own TTL circuits.

Charles Howerton has come up with an interesting and tightly coded package of 8080 routines to perform utility functions for applications software. The design goals of fitting into 256 bytes yet providing a wealth of extensions to the machine's instruction set are well met, as can be seen from his article's documentation of the package.

In the Queue

FEBRUARY 1977
Volume 2
Number 2 BYTE

Foreground

Background

Nucleus

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This month, for the first time, we run a guest editorial. The writer of this essay is Portia Isaacson, who is chairperson of the 1977 National Computer Conference which will be held in Dallas TX June 13-16 1977. (The conference this year for the first time recognizes the existence of our new trend in computing, personal computing, by creating a special theme for that purpose and taking the unprecedented step of adding a special exhibit hall for personal computing displays.) Here is an interesting view of the history and state of personal computing by an individual who has been enthusiastically participating right from the start. Portia is a professor of computer science at the University of Texas at Dallas and a principal in the Micro Store, a retail computer outlet located at 634 S Central Expressway, Richardson TX 75080, which is run by her husband David Wilson.

Personal Computing:

An Idea Whose Time Has Come!

Portia Isaacson, PhD
University of Texas at Dallas
Richardson TX 75080

It is clear that we are entering a dramatic new era in which information processing power will be abundantly available for use by the individual consumer...

Several years ago we knew that computers were going to become very small and very inexpensive. However, predictions of the effect of inexpensive computers did not begin to cover the strength of today's personal computing movement, where we find enthusiasm at a very high pitch. It is clear that we are entering a dramatic new era in which information processing power will be abundantly available for use by the individual consumer.

The only thing one could be sure about during the past year when writing about the personal computing movement is that by the time the article was printed it would certainly be antiquated. Every month there are several new computer clubs, several new computer stores, hundreds more computers owned by individuals, and a noticeably higher level of excitement among insiders to the movement. To most of us the whole idea of personal computing is so delightfully intoxicating that we can't quite believe its time has really come — but it has!

The personal computing movement started quietly enough when MITS announced a computer kit for under $500. Soon afterwards kits were available from several different manufacturers featuring the computer, a keyboard, a TV display interface, audio cassette interface, and the BASIC language; all for little more than $1,000. Wow! A really operational system for about the price of a good TV or stereo — clearly in personal range. So the hardware and BASIC software were available. The other needed ingredient was imagination.

There was no shortage of imagination. In fact, almost everyone who has ever worked with a computer has, at some time or another, been stricken with computeritis — the infection of the imagination with ideas about "what neat things could be done with a computer if only I had access." For years we've known that students many times substitute the computer center for other forms of recreational activity. Also, that many programmers can be found in the wee hours with their company computer, doing their own thing.

Applications of a personal computer are as far ranging as the individuals who imagine them. Personal accounting, music generation, library maintenance, language analysis, stock market analysis, game playing, model train control, household control, and tutoring are only a few of the known applications. The computer has few inherent limitations.

A "movement" can be characterized by the people involved. What kinds of people are "into" personal computing? And how many? Based on the circulation of the major personal computing publications and the attendance at conventions, 100,000 is surely a very conservative estimate of the rapidly growing number of involved people. What are these people like? True, at first, they

Continued on page 140

Introducing Sol Systems

A complete computer/terminal concept with all the standard features, software and peripheral gear you want in your personal computer.



Processor Technology Corporation


Sol Terminal Computer
OKIDATA 110
VDM DRIVER
Panasonic
Cobalt Energized
Tracs PLUS 40
Cobalt Energized
Tracs PLUS 40
OAE

Sol Systems put it all together. One source for hardware and software. One source for engineered compatibility of computer and peripherals. That's the Sol plan.

Though the microprocessor made the powerful small computer possible, a lot of folks found out early efforts in the marketplace were selling the sizzle a lot more than the steak. After an initial investment of several hundred dollars, you ended up with some nice parts, but no memory of any kind, no I/O devices or interfaces, no display, printout or software.

The Sol plan ends all that. Processor Technology takes the position that it's far better to be right than first. So let's get down to the Sol no tricks plan.

For $995 in kit form, the first complete small computer

Standard is a basic word at Processor Technology. The Sol-20 has more standard features than any other small computer we know of. Here's what you get.

8080 microprocessor* 1024 character video display circuitry* 1024 words of static low-power RAM* 1024 words of preprogrammed PROM* a custom, almost sensual 85-key solid-state keyboard* audio cassette interface capable of controlling two recorders at 1200 baud* both parallel and serial standardized interface connectors* a complete power supply* a beautiful case with solid walnut sides* software which includes a preprogrammed Prom personality module and a cassette with Basic-5 language plus two sophisticated computer video games* the ability to work with all S-100 bus (Altair 8800/IMSAI/PTC) products.

There are no surprises. Everything you need to make it work is here. In kit form, nominal assembly time from our fully documented instructions is four to seven evenings.

Or start with the Sol-PC for just $475

You can begin your Sol system with the all on one board Sol-PC kit. It has all the memory and interface electronics including video display, keyboard interface, audio cassette interface, all necessary software and the ability to accept the full Processor Technology line of memory and interface modules. Use the Sol-PC as the basis of a microcomputer, low cost CRT terminal or editing terminal

And these specs are standard

Display: 16 lines of 64 characters per line.
Character set: 96 printable ASCII upper and lower case characters plus 32 selectable control characters.
Display position: Continuously adjustable horizontally and vertically.
Cursor: Selectable blinking. Solid video inversion. Programmable positioning standard.
Serial interface: RS-232 and 20-mA current loop, 75 to 9600 baud, asynchronous.
Parallel interface: Eight data bits for input and output; output bus is tristate for bidirectional interfaces; levels are standard TTL.
Keyboard interface: Seven-level ASCII encoded, TTL levels.
Microprocessor: 8080, 8080A, or 9080A.
On-card memory: 1024 bytes PROM (expandable to 2048 bytes), 2048 bytes RAM.
External Memory: Expandable to 65,536 bytes total ROM, PROM, and RAM.
Video signal output: 1.0 to 2.5 volts peak-to-peak. Nominal bandwidth is 7 MHz.
Power required ($\pm 5\%$): +5 volts at 2.5 amperes, +12 volts at 150 mA, and −12 volts at 200 mA.

The Sol plan, completely expandable.

By filling the basic main frame with tailor made Processor Technology plug-in PC boards, you can really expand the computing power and flexibility of your Sol-20 Personal Computer.

New items are being announced frequently, but right now, here are some of the

things you can add to your Sol-20. The ALS-8 Firmware module is an assembly language operating system to give you the power to develop and run programs. Use it to quickly write, edit, assemble, de-bug and run your own programs. Some say it's the most useful software development on the market today, but modesty prohibits.

And when it comes to add-on memory boards, you've come to the right place. We've probably got more than anyone else. Choose from 2K ROM or 4, 8 or 16K RAM (read all about the 16KRA board on the last page of this ad). The PT 2KRO will accept up to eight 1702A or 5203Q erasable, reprogrammable memories (EPROM's) with the ability to store in a non-volatile fashion up to 2048 eight-bit words.

Our read/write memories are the industry standards for high reliability. We know, because we have literally scores of customer letters saying "Your memory modules work and keep on working."

To help you solve additional interfacing problems, add the 3P+S I/O module. Here's a board with two 8-bit parallel I/O ports with full handshaking logic and a serial data rate that can be set anywhere between 35 and 9600 baud. Set up control conditions for both parallel and serial ports. Data and error flags can be polled.

A full line of Sol-20 tailored peripherals

No computer can do the full job without the right set of peripheral gear. PT has sought out the best manufacturers of peripheral equipment and worked with them to give you a choice of quality so you can get the most out of your Sol-20. Choose from line and serial printers, perforated tape readers and punches, floppy disk memories, black and white or color graphics displays, A/D, D/A converters and more.

Software, the Computer Power Essential

A big part of making the first complete small computer is providing you with a wide range of easy to use, easy to obtain, low cost software. For the Sol-20, we've developed a whole group of offerings. And more are on their way.

TREK 80

Based on the NBC television series STARTREK, this 8K assembly language program uses the VDM graphics capability for real time war with the Klingons. No holds barred, they're out to get you from each of the 100 quadrants. TREK 80 resides and runs in 8K of memory and requires the PTC Sol or VDM-1.

New PT 8K Basic

Processor Technology has the fast new BASIC you've needed for so long. Using our superior BCD math, the speed of the new language is double that of our own fast BASIC-5. To multiple program capability, we've added strings, multidimensional arrays and multi-line, multi-variable, user functions. This is the BASIC for full capability systems. Look at the BUSINESS ANALYSIS program example in the manual to find out how PT 8K BASIC gives you more while using less memory for the working program.

Five reasons why it's so good

1. Strings are not limited to a length of 256 characters and can extend to the bounds of memory.
2. Renumbering of lines with full gosub, etc. updating. Also EXAM and FILL allow for direct memory operations while IN and OUT provide direct I/O capability.
3. Every statement is fully implemented. RESTORE, for instance, restores the data pointer as usual. BUT, with PT 8K BASIC, RESTORE 100 will set the pointer to the data located at line 100.
4. Fully implemented string and math functions include all of the standards — VAL, STR, ASC . . . . EXP and LOGI and LOG. Also, the more advanced statements such as ON-GOTO and IF THEN ELSE along with a loop EXIT are provided.
5. PT 8K BASIC has a 'perfect' implementation of PRINT USING which saves program memory space while still providing more capability than the usual PRINT USING.

The new PT 8K BASIC is similar to the version we're developing for ROM. You use it here before buying the more expensive ROM.

You'll find your PT 8K BASIC also includes both a built-in VDM driver and special editor. The cassette version also includes named program SAVE and LOAD for the CUTS Cassette interface or Sol.

New 8080 FOCAL™ DEC

8080 FOCAL has been updated to include operator precedence and all other standard FOCAL conventions. It also has a driver for VDM-1 display and PT Cassette program SAVE and LOAD This version is available only on CUTS Cassette and resides in 8K of memory.

GAMEPAC 1 to entertain family and friends

Show off your VDM-1 and computer with this lineup of video games. Each is included on the cassette or paper tape.

TARGET keeps track of your hits and misses while you blast away at the moving target. You and your family can get together for whole evenings at a time with this one.

ZING. Learn hexidecimal arithmetic fast with this VDM game as two players keep the five balls in the air. If both of you get too good . . . ZING, of course, will make it harder.

LIFE. The Sol or VDM makes a good display for the game of life and this version allows two modes of operation. The universe can be flat or wrapped around on itself. The real meaning of life we'll leave to you but it's fun to watch.

PATTERN. We haven't figured this one out ourselves but it's sure nice to have your computer doing it. You choose the geometric design and how rapidly it changes.

Sol Systems Price List

(prices are net, effective Dec. 1, 1976)

SOFTWARE **ITEM with manual**	**Source**	**CUTS cassette**	**Paper tape**
BASIC 5 software #2	**yes**	**	**$19.50**
8K BASIC	**no**	**$29.00**	**$37.00**
New 8080 Focal	**no**	**$14.50**	**N/A**
TREK 80 video game	**no**	**$ 9.50**	**$14.50**
GAMEPAC 1 video games	**no**	**$ 9.50**	**$14.50**
MATHPACK video calculator	**yes**	**$14.50**	**$19.50**
ASSEMBLER software #1	**yes**	**$14.50**	**$19.50**
ALS 8	**no**	**$35.00**	**$45.00**

**CUTS cassette of BASIC 5 is included FREE with all orders for Sol units or CUTS cassette interfaces. Additional cassettes available for $14.50.

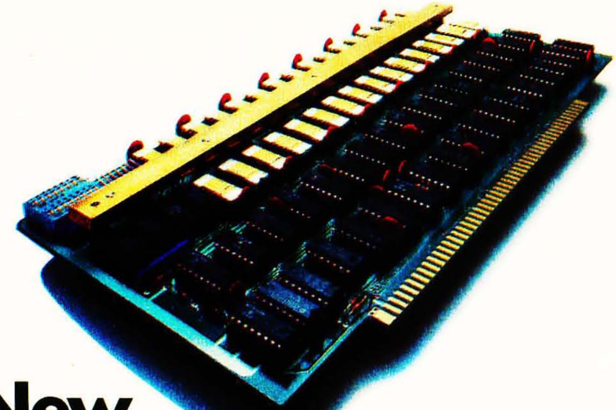
Sol system owners be sure to note Sol system on your order. These special versions use less code and provide easier loading along with more convenient operation. SOLOS, SOLED and CONSOL all have provision for the special versions.

Sol Terminal Computers	**Kit Price**
SOL-PC SINGLE BOARD TERMINAL COMPUTER™	**$475.***
SOL-10 TERMINAL COMPUTER™ Sol-PC with case, power supply and 70 key solid state keyboard.	**$795.***
SOL-20 TERMINAL COMPUTER™ all features of Sol-10 with larger power supply, 85 key solid state keyboard, fan, and five slot expansion backplane.	**$995.***

*Sol prices include CONSOL Personality Module. If SOLED Intelligent Editing Terminal Module or SOLOS Standalone Operating System Module is desired instead, add $100. If ordered separately, personality modules are $150 each.

Memory Modules	**Kit**	**Asmbld.**
ALS-8 PROM Resident Assembly Language Operating System	—	**$425**
SIM-1 Interpretive Simulator add-on option for ALS-8	—	**$ 95**
TXT-2 Text Editing add-on option for ALS-8	—	**$ 95**
2KRO Erasable PROM module	**$ 65**	**$ 89**
4KRA 4096-word Low Power Static RAM	**$159**	**$195**
8KRA 8192-word Low Power Static RAM	**$295**	**$375**
16KRA 16384-word Dynamic RAM	—	**$529**
Interface modules		
3P+S Parallel, Serial I/O module	**$149**	**$199**
CUTS Computer Users Tape System cassette interface	**$ 87**	**$119**
VDM-1 Video Display Module	**$199**	**$295**
Mass Storage Systems		
Helios II Disk System™ includes dual PerSci 270 floppy disk drive, cabinet, fan, S-100 bus compatible controller, power supply, system diskette with complete PTDOS software	**$1895**	**$2295**
Misc.		
EXB Extender Board	**$ 35**	**$ 45**
WWB Wire Wrap Board	**$ 40**	—

Prices, specifications and delivery subject to change without notice. Please allow up to two weeks for clearance of personal checks. Mastercharge accepted. All orders amounting to less than $30 must include $3 for handling.



New 16K RAM, fully assembled, $529

More bits per buck than ever before on a fully burned in and tested board unconditionally guaranteed for one year.

Processor Technology made the first 4K static RAM modules for the home computer market. Now in a price performance breakthrough we offer you a 16,384 byte dynamic memory module assembled, tested and burned in. Not a kit — and at $529 who'd want to build it from scratch?

Processor Technology gives you the features to make 4K dynamic RAMS work for you.

- Invisible refresh, no waiting while CPU is running.
- High speed 400 nsec access time worst case Z-80 and 8080 compatible.
- Versatile addressing, each 4096 byte segment is individually addressed to any of the sixteen available 4K segments.
- Low power — typically 5 watts when running — the same as most 4K memory modules.
- BATTERY BACKUP capability built-in for standby operation.
- IMPORTANT NOTICE — No 16K memory module available is fully, truly static. 4200/4402 type "static" RAM's have high level, high current clocks with high transient power levels. Any RAM with 12 volt 30 mA clock pulses should not be called "STATIC" just because each memory cell is a flip-flop.

Specifications

Access Time	400 nsec max
Cycle Time	500 nsec max
Rams Used	Intel 2104 or Mostek 4096 types
Capacity	16384 8-bit bytes
Memory Protect	standard on card
Addressing	each 4096 byte page addressable
Operating Power	+7.5 to 10 VDC at 0.4 A typical +15 to +18 V at 100 mA typical −15 to −18 VDC at 20 mA max

See your nearest dealer listed below or contact us directly. Address Processor Technology, 6200 Hollis Street, Emeryville CA 94608, Phone 415/652-8080.

Processor Technology Dealers

CALIFORNIA

The Byte Shop
1514 University Ave.
Berkeley CA 94703

The Byte Shop
2559 South Bascom Ave.
Campbell CA 95008

The Computer Mart
624 West Katella #10
Orange CA 92667

The Byte Shop
2227 El Camino Real
Palo Alto CA 94306

The Computer Center
8205 Ronson Road
San Diego CA 92111

The Computer Store
of San Francisco
1093 Mission Street
San Francisco CA 94103

The Byte Shop
509 Francisco Blvd.
San Rafael CA 94901

The Byte Shop
3400 El Camino Real
Santa Clara CA 95051

The Byte Shop
2989 North Main St.
Walnut Creek CA 94596

FLORIDA

Microcomputer
Systems Inc.
144 So. Dale Mabry Hy.
Tampa FL 33609

GEORGIA

Atlanta Computer Mart
5091-B Buford Hwy.
Atlanta GA 30340

ILLINOIS

The Numbers Racket
518 East Green Street
Champaign IL 61820

itty bitty
machine co., inc.
1316 Chicago Ave.
Evanston IL 60201

The Chicago
Computer Store
517 Talcott Road
Park Ridge IL 60068

INDIANA

The Data Domain
111 South College Ave.
Bloomington IN 47401

MICHIGAN

The Computer Store
of Ann Arbor
310 East Washington
Ann Arbor MI 48104

NEW JERSEY

The Computer Mart
of New Jersey
151 Kline Boulevard
Colonia NJ 07067

Hoboken Computer Works
56 Second Street
Hoboken NJ 07030

NEW YORK

Audio Design Electronics
487 Broadway, Ste. 512
New York NY 10013

The Computer Corner
200 Hamilton Ave.
White Plains NY 10601

The Computer Mart
of Long Island
2072 Front Street
East Meadow, L.I. NY 11554

The Computer Mart
of New York
314 Fifth Ave.
New York NY 10001

Synchro Sound Enterprises
193-25 Jamaica Ave.
Hollis NY 11423

OREGON

The Real Oregon
Computer Co.
205 West 10th Ave
Eugene OR 97401

RHODE ISLAND

Computer Power, Inc.
M24 Airport Mall
1800 Post Road
Warwick RI 02886

TEXAS

The Micro Store
634 South Central
Expressway
Richardson TX 75080

WASHINGTON

The Retail Computer Store
410 N.E. 72nd
Seattle WA 98115

WISCONSIN

The Milwaukee Computer Store
6919 W. North Ave.
Milwaukee WI 53213

CANADA

The Computer Place
186 Queen St. West
Toronto, Ontario M5V 1Z1

Trintronics
160 Elgin St.
Ottawa, Ontario

Processor Technology Corporation

Letters

SAVE THE COMPUTERS FOUNDATION?

As a regular reader of the articles in BYTE magazine I have noticed the absence of any columns on computer nostalgia and antique computers. Antique computer interest appears to be growing because it is perceived in perspective to and in contrast with microprocessors. Nostalgia discussions would compare old computers with microcomputers in the area of first cost, computing power, logical organization, speed, electricity consumption, size, weight, reliability, etc.

Antique computers include the desk size drum and vacuum tube machines of the 50s, early magnetic core minis of the 60s, and the first Wang and HP desk top calculators of the late 60s. The oldest antique computers include the Royal-McBee LGP-30, Bendix G-15, Burroughs E101, IBM 650, Elcon 125, Alwac, Monrobot VI, Univac I and II, and the IBM 700 and 7000 series.

Since only a few of these machines were ever built, and many have already disappeared, there is a real danger they may become extinct. We can help preserve our computer heritage by publishing interesting articles on computer nostalgia and antique computers.

Don Nyre
305 LaJolla Dr
Newport Beach CA 92663

Only problem: You can only look at 'em, because the power bills will be sky high, and who has used vacuum tubes for spare parts? Interested readers are urged to contact Don, or write up commentary on their favorite antiques so we can occasionally publish some history. Who'll write an account of Babbage's engine?

ARE WE SCHIZOPHRENIC PLUGGED-IN EXPERIMENTALISTS?

I just scanned issue No. 14 and am well pleased! BYTE seems to give the same schizophrenic, plugged-in, experimentalist joy of ham radio's old days before commercial (yawn) availability of 2000 watt PEP linear amplifiers. This is the impetus, battered and bruised by a nasty electrical engineering curriculum, jaded by very large scale integration, which has largely failed me these days.

Before I go back to working on my business and law school applications, let me give *you* a reason for joy: money! Please note the gift subscription form and the address label upon this sleeve. I'd like to buy a year's subscription for my friend and three years for myself.

Jeffrey S Wilson
POB 30113
Parma Heights OH 44130

The above letter was written on a battered BYTE wrapper.

I DON'T LIKE YOUR PRODUCT

Please do not send me any more issues of BYTE. I got the first two issues and did not like it. I got the impression the magazine was intended for computer hobbyists. Instead, it seems to me more dreary and boring than any textbook or trade journal today. I have been a computer professional for fifteen years, and your publication is by far the dullest I've seen. Let me know if your format or content changes in the future. Meanwhile, no more issues please.

Ray Lawrence
120 Roseland La
East Patchogue NY 11772

Congratulations, Ray. You've just exercised your right to vote your preferances in a free market, by what you buy and what you don't buy. We'll collect our votes from the remaining 73,000 or so people (circa January 1977 issue) who don't seem to feel the way you do.

TELE SELECTRIC CONVERSIONS?

Recently I have a project in mind to build an intelligent teleprinter. The system will consist of a converted electric typewriter which will be controlled by a 8080A microprocessor, 8 K memory and 3 programmable IO ports which includes RS232 interface. The advantage of this teleprinter is that it can be used as a stand alone computer or as a computer terminal.

The typewriter I intend to use is the

Continued on page 76

How come the master of this machine has to be relegated to such a menial task as remembering to enter line numbers?

Sweet Auto Line



Willard I Nico
DELTA t
11020 Old Katy Rd, Suite 204
Houston TX 77043

I was writing a program the other day, using the editor and assembler provisions of the SYS 8 self-contained operating system. For the N to the ith time, I forgot to type in a new line number before entering the instruction code and got the familiar WHAT? response from the monitor program. If there was a market for WHAT?, I'd be rich!

Anyway, the thought hit me like a brick, "How come the master of this machine has to be relegated to such a menial task as remembering to enter line numbers?" After all, my IMSAI is supposed to be the kind of a servant who doesn't mind that type of work. I should be free to think creatively. That's when I decided to put SAL on the payroll: my Sweet Auto Line automatic line numbering program.

Original SYS8

```
READ:   LXI H,IBUF
        SHLD  ADDS
        MVI E,2
NEXT:   CALL  IN8
```

Modified SYS8

```
READ:   LXI H,IBUF
        JMP   PATCH
BACKIN: MVI E,2
NEXT:   CALL  IN8
```

SAL Patch

```
PATCH: SHLD  ADDS
       JMP   [ ][ ]
```

ONOFF, a switch location with address of AUTOL if SAL is on, address of BACKIN if SAL is off

thus if SAL is on the code is

```
PATCH: SHLD  ADDS
       JMP   AUTOL
```

thus if SAL is off the code is

```
PATCH: SHLD  ADDS
       JMP   BACKIN
```

Listing 1: Change that must be made to the SYS 8 monitor input logic in order to determine whether or not the auto line indexing feature is wanted.

In any problem, the first step is to decide what the problem is. . .

Job Description

The first step was to decide exactly what was required, and I came up with the following list:

1. Automatically generate a four digit number at the beginning of each data file line.
2. Allow for selection of the increment of increase between line numbers.
3. Permit manual entry of out of sequence line numbers to allow program correction.
4. Allow the automatic feature to be turned on and off as desired.
5. Provide for selection of the beginning line number.
6. Automatically disable the feature when an executive command is entered.

After fiddling with the ideas and writing the program, I now have Sweet Auto Line working for me and I don't forget to enter line numbers any more. In fact, I don't even think about them; SAL and IMSAI do it for me.

The starting point for writing the Sweet Auto Line program was to define exactly how SYS 8 handles data input from the keyboard. Figure 1 is a flowchart detailing the procedure used in this 8080 monitor and where my Sweet Auto Line routines are patched into it. The flowchart shows that the program does not carry out any processing of the input information until the entire line has been entered. Each character typed in is stored in sequential locations of the IBUF input buffer until the carriage return code (ASCII hexadecimal 0D) is detected. This code signals the monitor that input of data for the current line is complete.

The monitor then examines the first character in IBUF to determine if it is a numeral. Lines beginning with one of the numbers 0 through 9 are flagged as program lines for the current file. If the first character in IBUF is other than a number, the program branches to the executive area.

Sweet Auto Line depends on a SYS 8 convention for proper operation: At least one space character must be entered after a

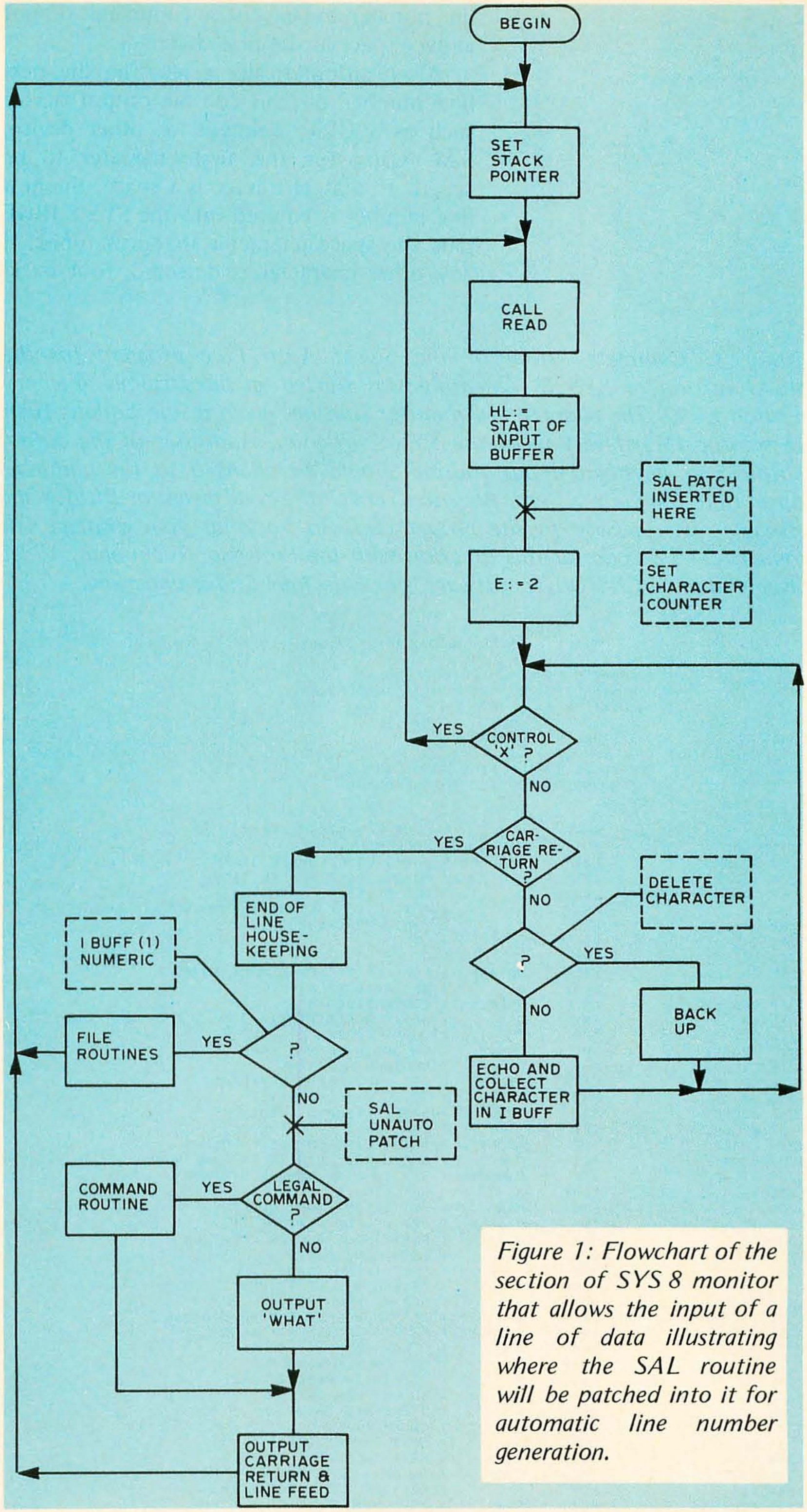


Figure 1: Flowchart of the section of SYS 8 monitor that allows the input of a line of data illustrating where the SAL routine will be patched into it for automatic line number generation.

```
Original SYS8                    Modified SYS8                    SAL Patch

SYS8:  LXI   SP,AREA+18          SYS8:  LXI   SP,AREA+18          UNAUTO:  LXI   H,BACKIN
       CALL  READ                       CALL  READ                         SHLD  ONOFF
       INX   H                          INX   H                            CALL  COMM
       MOV   A,M                        MOV   A,M                          JMP   EOR
       CPI   '9'+1                      CPI   '9'+1
       JC    LINE                       JC    LINE
       CALL  VALC                       CALL  VALC
       CALL  COMM                       JMP   UNAUTO
EOR:   CALL  CRLF                EOR:   CALL  CRLF
       JMP   SYS8                       JMP   SYS8
```

Listing 2: Change in the original SYS 8 system that allows the SAL patch to be turned off again.

line number and executive commands do not allow a space as the first character.

After automatically generating the new line number on the console output device such as a CRT, Teletype or other device, SAL waits for the first character to be typed. If that character is a space, the new line number is entered into the SYS 8 IBUF plus the space character that was typed. If any other character is detected, four backspace commands are output to the console to wipe out the line number and the typed character is entered as the first one in IBUF. After each line number is entered in IBUF, it is increased by the operator selected increment and saved for use in the next program line.

Turning on SAL

The initial line number is established by using a SETL executive command with parameter passing. The technique for adding your own executive commands, such as SETL, was described in the January 1977

Listing 3: Complete listing of the Sweet Auto Line program for the IMSAI version of SYS 8. Assembly was started at hexadecimal memory location E200. The addresses of monitor routines given in the Equate Table are for the IMSAI version of the SYS 8 program. Addresses of the output routine and keyboard input routine should be changed to the addresses appropriate for your system. Be sure to check the code given for BKSPA and change it if necessary to the proper code to back up your display. The standard SYS 8 code for this function with the Processor Technology Video Display Module CRT Driver software is hexadecimal 5F for underline.

```
                        TITLE    'SWEET AUTO-LINE  -  By Willard I. Nico'
                ;
                ; AUTOMATIC LINE NUMBERING PROGRAM
                ; FOR MICROTEC "SYS 8" MONITOR/ASSEMBLER
                ; By Willard I. Nico
                ;
E200                    ORG     0E200H
                ;
                ; THE ABOVE INSTRUCTION ESTABLISHES
                ; THE ADDRESS AT WHICH THIS PROGRAM
                ; BEGINS.
                ;
E200 E5         AUTOL:  PUSH    H       ; SAVE H & L REGISTERS
E201 0E02               MVI     C,2     ; LOOP COUNTER
E203 21CAE2             LXI     H,NUMBR ; ASCII LINE NUMBER STASH
E206 11C7E2             LXI     D,LINE  ; BINARY LINE NUMBER STASH
E209 1A         CONVT:  LDAX    D       ; GET BYTE
E20A 0F                 RRC             ; ROTATE MOST SIGNIFICANT BITS
E20B 0F                 RRC             ;  INTO POSITION
E20C 0F                 RRC             ;
E20D 0F                 RRC             ;
E20E CDAAE2             CALL    UNPACK  ; CONVERT PACKED BINARY TO ASCII
E211 1A                 LDAX    D       ; GET BYTE BACK
E212 CDAAE2             CALL    UNPACK  ; CONVERT AGAIN
E215 13                 INX     D       ; NEXT PACKED DIGIT
E216 0D                 DCR     C       ; COUNT LOOPS
E217 C209E2             JNZ     CONVT   ; GO AGAIN IF NOT DONE
E21A E1                 POP     H       ; RESTORE REGISTERS
E21B CD06D8             CALL    KBDIN   ; GET INPUT FROM KEYBOARD
E21E 78                 MOV     A,B     ; MOVE TO ACCUMULATOR
E21F 32C9E2             STA     SAVE    ; SAVE KEYBOARD INPUT
E222 FE20               CPI     ' '     ; WAS INPUT A 'SPACE'?
E224 C24EE2             JNZ     ABORT   ; NOT A LINE FOR FILE IF NOT
E227 0E04               MVI     C,4     ; OK TO GO.  DIGITS IN LINE NUMB
E229 11CAE2             LXI     D,NUMBR ; SET TO LINE NUMBER STORAGE
E22C 1A         LOOP2:  LDAX    D       ; GET DIGIT
E22D 77                 MOV     M,A     ; PUT IT IN INPUT BUFFER
E22E 13                 INX     D       ; SET UP FOR NEXT DIGIT
E22F 23                 INX     H       ; NEXT INPUT BUFFER LOCATION
E230 0D                 DCR     C       ; COUNT THE DIGIT
E231 C22CE2             JNZ     LOOP2   ; LOOP IF NOT DONE
E234 E5                 PUSH    H       ; SAVE H & L REGISTERS
E235 0E02               MVI     C,2     ; SET UP COUNTER
E237 11C8E2             LXI     D,LINE+1; SET TO PACKED NUMBER STORAGE
E23A 21CFE2             LXI     H,INCR+1; SET TO INCREMENT VALUE
E23D AF                 XRA     A       ; CLEAR CARRY
E23E 1A         LOOP1:  LDAX    D       ; GET PACKED NUMBER
E23F 8E                 ADC     M       ; ADD IN INCREMENT VALUE
E240 27                 DAA             ; ADJUST FOR DECIMAL
E241 12                 STAX    D       ; STORE NEW VALUE
E242 0D                 DCR     C       ; COUNT IT
E243 1B                 DCX     D       ; NEXT PACKED DIGIT
E244 2B                 DCX     H       ; NEXT INCREMENT VALUE
E245 C23EE2             JNZ     LOOP1   ; DO NEXT IF C NOT AT ZERO
E248 E1                 POP     H       ; RESTORE H & L REGISTERS
E249 1E06               MVI     E,6     ; TELL MONITOR 5 CHARACTERS
E24B C35BE2             JMP     DONE    ; GO FINISH
E24E 0E04       ABORT:  MVI     C,4     ; NOT A PROGRAM LINE. ERASE
E250 0608       LOOP4:  MVI     B,BKSPA ; LOAD BACKSPACE CODE
E252 CD00E0             CALL    CRTOUT  ; BACK UP LINE NUMBER ON CRT
E255 0D                 DCR     C       ; COUNT IT
E256 C250E2             JNZ     LOOP4   ; LOOP IF NOT DONE
E259 1E02               MVI     E,2     ; TELL MONITOR ABOUT INPUT CHAR.
E25B 3AC9E2     DONE:   LDA     SAVE    ; GET THE KEYBOARD INPUT
E25E C3CC00             JMP     NEXT+4  ; GO TO MONITOR
                ;
                ; THIS PORTION OF THE PROGRAM SETS THE
                ; STARTING LINE NUMBER AND THE INCREMENT
                ; VALUE
                ;
E261 210005     SETL:   LXI     H,0500H ; DEFINE DEFAULT INCREMENT=5
E264 22CEE2             SHLD    INCR    ; STORE DEFAULT INCREMENT
E267 CD3303             CALL    VCHK    ; CHECK PARAMETER ENTERED
E26A 21C7E2             LXI     H,LINE  ; SET TO CURRENT LINE NO. STASH
```

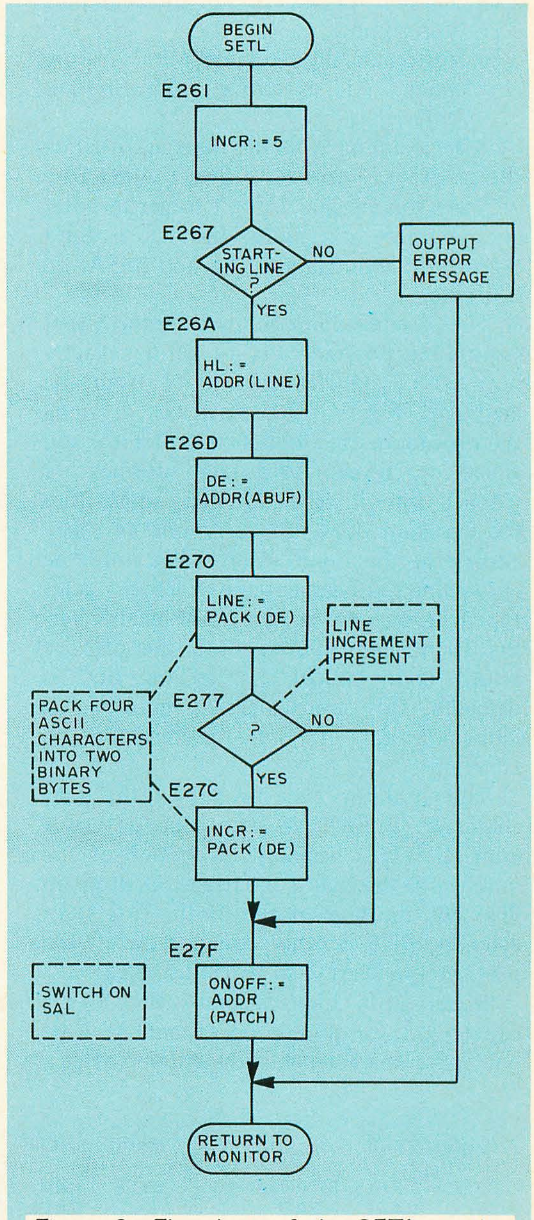
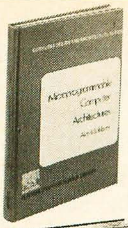
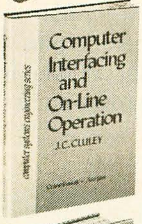


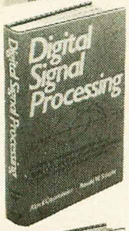
Figure 2: Flowchart of the SETL routine that will determine at what number the line numbers should begin and what the increment between line numbers will be. Addresses in this figure refer to listing 3.



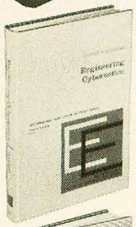
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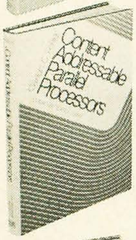
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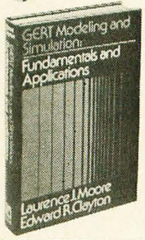
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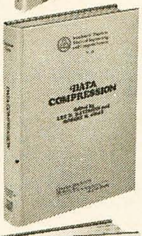
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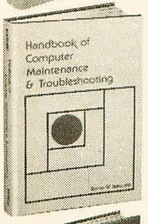
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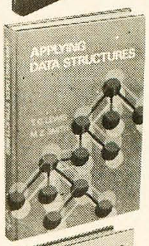
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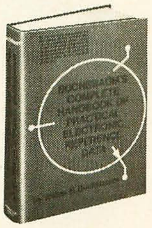
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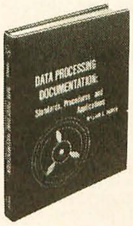
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Listing 3, continued:

```
E26D 117E10            LXI     D,ABUF  ; SET TO ASCII BUFFER
E270 CD88E2            CALL    PACK    ; PACK BCD DIGITS
E273 21CEE2            LXI     H,INCR  ; SET TO INCREMENT STORAGE
E276 1A                LDAX    D       ; GET FIRST VALUE FROM ABUF
E277 FE00              CPI     0       ; CHECK IF INCREMENT ENTERED
E279 CA7FE2            JZ      SWITCH  ; USE DEFAULT VALUE IF NOT
E27C CD88E2            CALL    PACK    ; PACK INCREMENT VALUES
                ;
                ; THIS PORTION OF THE PROGRAM CHANGES
                ; THE DESTINATION OF THE JUMP INSTRUCTION
                ; IN THE PATCH TO ACTIVATE THE AUTOMATIC
                ; LINE NUMBERING FEATURE
                ;
E27F 2100E2     SWITCH: LXI    H,AUTOL ; START ADDRESS OF AUTOL ROUTINE
E282 22B9E2            SHLD    ONOFF   ; STORE IT AT BRANCH LOCATION
E285 C3BA00            JMP     EOR     ; RETURN TO MONITOR INPUT
                ;
                ; THE FOLLOWING SUBROUTINE PACKS
                ; FOUR ASCII DIGITS INTO TWO
                ; EIGHT-BIT BINARY BYTES
                ;
E288 CD8BE2     PACK:   CALL   TWICE   ; DO FOLLOWING ROUTINE TWICE
E28B CD9CE2     TWICE:  CALL   TEST    ; TEST FOR NUMERICAL DIGIT
E28E 07                RLC             ; ROTATE BITS TO LEFT
E28F 07                RLC             ;  FOUR BITS OF PACKED
E290 07                RLC             ;  BINARY
E291 07                RLC             ;  BYTE
E292 47                MOV     B,A     ; HOLD
E293 13                INX     D       ; SET TO NEXT DIGIT
E294 CD9CE2            CALL    TEST    ; CHECK LEGAL DIGIT
E297 80                ADD     B       ; PACK 2 DIGITS
E298 77                MOV     M,A     ; STORE RESULT
E299 13                INX     D       ; SET TO NEXT DIGIT
E29A 23                INX     H       ; NEXT STORAGE LOCATION
E29B C9                RET
                ;
                ; THIS SUBROUTINE TESTS AN ASCII CHARACTER
                ; TO MAKE SURE IT IS ONE OF THE DIGITS
                ; "0" THROUGH "9".  IF IT IS NOT,
                ; AN EXIT IS MADE TO THE ERROR ROUTINE.
                ; THE ASCII NUMBER CODE IS ALSO
                ; STRIPPED FROM THE CHARACTER
                ;
E29C 1A         TEST:   LDAX   D       ; GET DIGIT
E29D FE30              CPI     '0'     ; ASCII 0 OR HIGHER
E29F DAA504            JC      WHAT    ; ERROR IF NOT
E2A2 FE3A              CPI     ':'     ; CAN'T BE MORE THAN 9
E2A4 D2A504            JNC     WHAT    ; ERROR IF SO
E2A7 E60F              ANI     0FH     ; STRIP OFF ASCII CODE
E2A9 C9                RET
                ;
                ; THIS SUBROUTINE UNPACKS AN EIGHT-BIT
                ; BINARY BYTE INTO TWO ASCII NUMERICAL
                ; CHARACTERS
                ;
E2AA E60F       UNPACK: ANI    0FH     ; MASK ALL BUT FOUR BITS
E2AC C630              ADI     '0'     ; ADD ASCII NUMBER CODE
E2AE 77                MOV     M,A     ; STORE AS ASCII
E2AF 47                MOV     B,A     ; HOLD IN B REGISTER
E2B0 CD00E0            CALL    CRTOUT  ; ECHO TO OUTPUT
E2B3 23                INX     H       ; SET TO NEXT STORAGE LOCATION
E2B4 C9                RET
                ;
                ; THE FOLLOWING ROUTINE IS THE PATCH
                ; THAT CONTROLS WHETHER OR NOT AUTOMATIC
                ; LINE NUMBERS ARE GENERATED
                ;
E2B5 227410     PATCH:  SHLD   ADDS    ; ORIGINAL SYS 8 INSTRUCTION
E2B8 C3                DB      0C3H    ; JUMP INSTRUCTION
E2B9 C700       ONOFF:  DW     NEXT-1  ; DEFINE AS OFF INITIALLY
                ;
                ; THIS ROUTINE TURNS AUTOMATIC
                ; LINE NUMBERING FEATURE OFF
                ;
E2BB 21C700     UNAUTO: LXI    H,NEXT-1; MONITOR IS DESTINATION IF "OFF
E2BE 22B9E2            SHLD    ONOFF   ; STORE DESTINATION IN PATCH
E2C1 CD5E01            CALL    COMM    ; ORIGINAL SYS 8 INSTRUCTION
E2C4 C3BA00            JMP     EOR     ; RETURN TO MONITOR
                ;
                ; THIS IS THE AREA WHERE THE PROPER ADDRESSES
                ; ARE STORED FOR THE VARIOUS LOCATIONS
                ; REFERENCED IN THE AUTOL PROGRAM
                ;
E2C7            LINE:   DS     2       ; STASH FOR CURRENT LINE NUMBER
E2C9            SAVE:   DS     1       ; STORAGE FOR KEYBOARD INPUT
E2CA            NUMBR:  DS     4       ; STASH FOR ASCII LINE NO.
E2CE            INCR:   DS     2       ; STASH FOR INCREMENT VALUE
E000            CRTOUT  EQU    0E000H  ; VIDEO DRIVER PROGRAM
0008            BKSPA   EQU    08H     ; BACKSPACE CODE OF VIDEO DRIVER
D806            KBDIN   EQU    0D806H  ; ADDRESS KEYBOARD INPUT ROUTINE
107E            ABUF    EQU    107EH   ; ASCII BUFFER ADDRESS
0333            VCHK    EQU    0333H   ; VCHK ROUTINE IN MONITOR
00BA            EOR     EQU    00BAH   ; MONITOR INITIALIZATION
00C8            NEXT    EQU    00C8H   ; MONITOR REENTRY POINT
04A5            WHAT    EQU    04A5H   ; ERROR MESSAGE
015E            COMM    EQU    015EH   ; MONITOR COMMAND SEARCH
1074            ADDS    EQU    1074H   ; MONITOR STORAGE LOCATION
                ;
                ; END OF PROGRAM
                ;
                       END

ABORT E24E      ABUF  107E      ADDS  1074      AUTOL E200
BKSPA 0008      COMM  015E      CONVT E209      CRTOU E000
DONE  E25B      EOR   00BA      INCR  E2CE      KBDIN D806
LINE  E2C7      LOOP1 E23E      LOOP2 E22C      LOOP4 E250
NEXT  00C8      NUMBR E2CA      ONOFF E2B9      PACK  E288
PATCH E2B5      SAVE  E2C9      SETL  E261      SWITC E27F
TEST  E29C      TWICE E28B      UNAUT E2BB      UNPAC E2AA
VCHK  0333      WHAT  04A5
```

issue of BYTE under the title "SYS 8½ . . . Your Own Executive Commands," page 66.

The command format is: SETL 0100 10

In this example, the first program line number will be 0100, the second 0110, and so on with each line number being 10 higher than the preceeding one. The SETL subroutine accepts input of the initial line number you wish SAL to generate, plus the increment by which each succeeding line number is to increase. The program checks

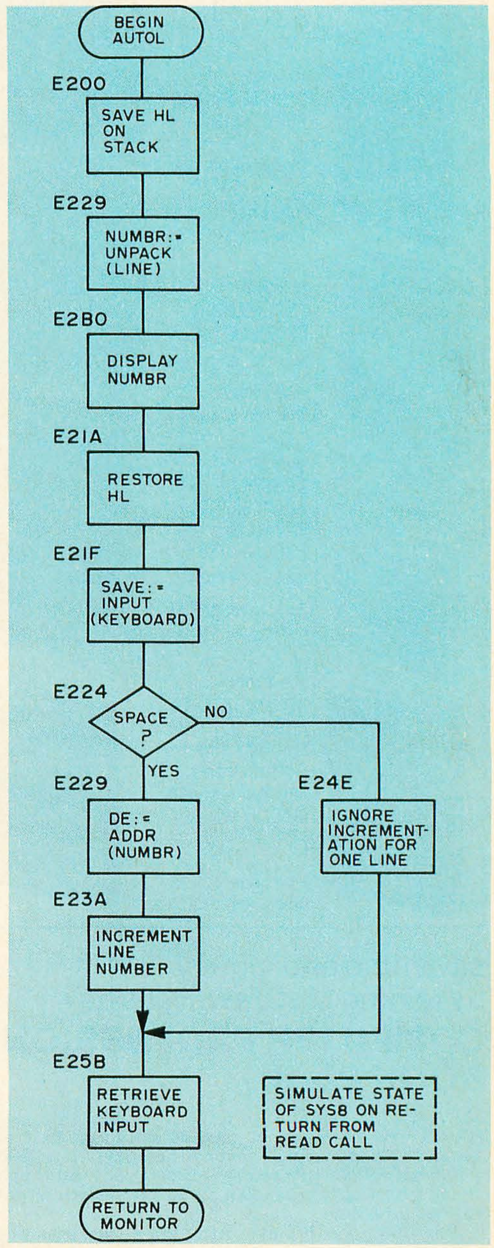


Figure 3: Flowchart of the AUTOL routine that increments the line numbers and determines if an executive command has been entered. If an executive command is input the automatic line numbering will cease. Addresses in this figure refer to listing 3.

to make sure you entered the starting number by using the VCHK routine in SYS 8. If you forgot to enter the number, you get another WHAT? for your collection. If an increment value is not entered, the default value of 5 is used. Sweet Auto Line is activated when the SETL command is issued and deactivated by the use of any other executive command.

Employer Provided Tools

To get SAL working productively, you need to provide the proper working environment. What your new employee needs are two small changes to the SYS 8 program and, of course, the Sweet Auto Line program itself.

The first change to SYS 8, shown in listing 1, diverts program flow to a patch in Sweet Auto Line that determines if the automatic feature is on or off. The patch contains the line of code which was replaced in the monitor plus a JMP instruction. The second and third bytes of the JMP instruction are changed by SETL so that the destination of the jump is AUTOL, the start of the line numbering program. This turns SAL on.

The second change to SYS 8, shown in figure 3, is similar except that program flow is diverted to the UNAUTO routine in SAL. UNAUTO changes bytes two and three of the JMP instruction in the patch so that the program goes right back where it came from without going through the line numbering procedure. This turns SAL off.

Method to Madness Dept

Here's why the particular locations for changes to the monitor were chosen.

Each new line of data input begins at READ call in the monitor. First, we allow the HL register pair to be set to the start of the input buffer by the LXI H, IBUF instruction. Our JMP to the patch replaces the SHLD ADDS instruction. If SAL is off, the program flow jumps back to the MVI E, 2 instruction and everything works as though there had been no changes at all.

However, if SAL is on, the line number will be automatically placed in IBUF, the character counter, register E, will be set to the correct value, and the first keyboard input character will be in resister A. The return will be to the CPI 24 instruction.

The jump to UNAUTO replaces the CALL to COMM which is duplicated in the UNAUTO routine. If a line of input data does not start with a number, the program flows through UNAUTO to turn SAL off before checking for a legal executive command.

Note: The SYS 8 Monitor/Editor/Assembler was written by Microtec of Sunnyvale CA, and is included free with the IMSAI 8080 Computer. Processor Technology Co distributes a similar version of the same program for only a copying charge.

Put SAL to Work

When using SAL, an executive command is used to set the beginning line number, optionally select the increment of increase for each succeeding line, and turn SAL on. This command and the address of the SETL routine should be added to your executive command table. The command is:

SETL beginning-line [increment]

(square brackets denote options)
Examples:

	First Line No.	Increase
SETL 1000 20	1000	20
SETL 1 5	0001	5
SETL 20	0020	5
SETL A100 10	WHAT?	

To turn SAL off, use any executive command, even one that is not in CTAB. Of course, you can't use SETL!

To correct a previous line, simply follow the standard procedure and type in the line number you wish to correct. When finished, SAL will repeat the line number she has saved as next. If you forget to type a space after SAL delivers the line number, use the key you would normally use to back up, usually the underline. When you have backed up to the beginning of the line, type a carriage return and SAL will repeat the next line number.

Note that the maximum line number that SYS 8 can handle is 9999. SAL makes no test that this number has been exceeded. The next number after 9999 is 0000 and if you are not careful you may write over some of your program lines. The line increment value may range from 0 to 9999. If you use 0, you will set the same line number over and over. If you use 9999, well, would you believe a two line program?

How Does She Do It?

SAL uses four locations to store various data. These are:

LINE	2 bytes for the next line number in packed binary format
SAVE	1 byte for the keyboard input character
NUMBR	4 bytes for the next line number in ASCII format
INCR	2 bytes for the increase increment in packed binary format

The first program activity occurs when the beginning line number and increment are set and SAL is turned on. Those functions are handled by the SETL routine as shown in the flowchart in figure 2. In the event no increment is specified, the default value of 5

Listing 4: Equate Table with monitor routine addresses for using the Sweet Auto Line program with the Processor Technology version of the SYS 8 program. This assembly was started at hexadecimal memory location 5000.

```
        ; THIS IS THE AREA WHERE THE PROPER ADDRESSES
                ; ARE STORED FOR THE VARIOUS LOCATIONS
                ; REFERENCED IN THE AUTOL PROGRAM
                ;
50C7            LINE:   DS      2       ; STASH FOR CURRENT LINE NUMBER
50C9            SAVE:   DS      1       ; STORAGE FOR KEYBOARD INPUT
50CA            NUMBR:  DS      4       ; STASH FOR ASCII LINE NO.
50CE            INCR:   DS      2       ; STASH FOR INCREMENT VALUE
E000            CRTOUT  EQU     0E000H  ; VIDEO DRIVER PROGRAM
0008            BKSPA   EQU     08H     ; BACKSPACE CODE OF VIDEO DRIVER
D806            KBDIN   EQU     0D806H  ; ADDRESS KEYBOARD INPUT ROUTINE
D05A            ABUF    EQU     0D05AH  ; ASCII BUFFER ADDRESS
F293            VCHK    EQU     0F293H  ; VCHK ROUTINE IN MONITOR
F01F            EOR     EQU     0F01FH  ; MONITOR INITIALIZATION
F02D            NEXT    EQU     0F02DH  ; MONITOR REENTRY POINT
F41A            WHAT    EQU     0F41AH  ; ERROR MESSAGE
F0C3            COMM    EQU     0F0C3H  ; MONITOR COMMAND SEARCH
D050            ADDS    EQU     0D050H  ; MONITOR STORAGE LOCATION
                ;
                ; END OF PROGRAM
                ;
                        END
```

is used. This value is loaded into the HL register pair and stored at INCR at the start of SETL. If a later test shows that a different value is desired, INCR is changed accordingly.

Next, the monitor's VCHK routine is used to determine if a beginning line number was specified. VCHK exits to the WHAT? error routine if it finds no line number was chosen. If a line number is found, the HL resister pair is set to the LINE storage area and the DE register pair is loaded with the address of the monitor's ASCII buffer, ABUF. The first four ASCII digits in ABUF are converted to simple binary values and then packed two to a byte by the PACK routine. Each digit is tested to make sure it is a valid number by TEST. The two bytes are then stored at LINE.

SETL then checks the next ABUF entry for an increment value. If none is present, the 5 initially stored is used. If an entry is found, the next four ABUF characters are packed into two bytes as before and stored in INCR.

The SWITCH routine fetches the starting address of the AUTOL routine and stores it as the second and third bytes of the jump instruction in PATCH, thus turning SAL on. Each time the monitor enters its READ routine, the program is diverted to SAL's PATCH. If SAL is on, the program goes through AUTOL to generate a line number.

As the flowchart of figure 3 shows, AUTOL saves the data in the HL register pair on the stack so that those registers are available for use. They are then set to the address of the NUMBR storage area. Register pair DE is set to the LINE memory address and the next line number is retrieved from that area and unpacked into four ASCII digits. The UNPACK routine stores the ASCII digits in the NUMBR stash and, as each digit is stored, it is also displayed on the console device.

After displaying the line number, the program waits for an input from the keyboard which it stores in the SAVE memory byte. This input is tested for a space and if it is any other character, a jump to the ABORT routine cancels the entry of the line number into the monitor's input buffer. If a space is detected, the ASCII digits in the NUMBR stash are entered into the monitor's input buffer, IBUF. The value stored in INCR is then added to the line number in LINE and the new value restored in LINE for use the next time through.

The E register is used by the monitor to point to the place in IBUF just after the last valid character. Since we have added a four digit line number plus a keyboard entry character, we set register E to 6 so that the monitor knows what we have done. Lastly, the keyboard character is retrieved from SAVE and carried back to the monitor for input of the rest of the line.

In the ABORT portion of the program, four rubout commands are generated to wipe out the line number printed on the control console. Since the number had not been entered into IBUF or increased by the increment value when the nonspace keyboard entry was detected, no further processing of the line number is necessary. The E pointer register is set to 2 to indicate that one character is in IBUF, the SAVEd character retrieved and the monitor reentered. The PACK routine extracts the binary equivalents of ASCII numbers and combines two of them into one byte. This packing facilitates adding the increment value to the line number by allowing use of the DAA, Decimal Adjust Accumulator instruction. PATCH, SWITCH and UNAUTO have already been explained in sufficient detail.

A program listing of the Sweet Auto Line is shown in listing 3. The addresses of the monitor routines given in the Equate Table are for the IMSAI version of the SYS 8 program. If you are using the Processor Technology version of this program the appropriate addresses can be found in listing 4.

Well, there you have it! Sweet Auto Line is an example of sane, moderately intricate computer programming which goes to work and makes life easier for you. You will find it convenient to use, and after a short while, you'll wonder how you ever got along without SAL on the payroll.

Now if she could just type . . .■

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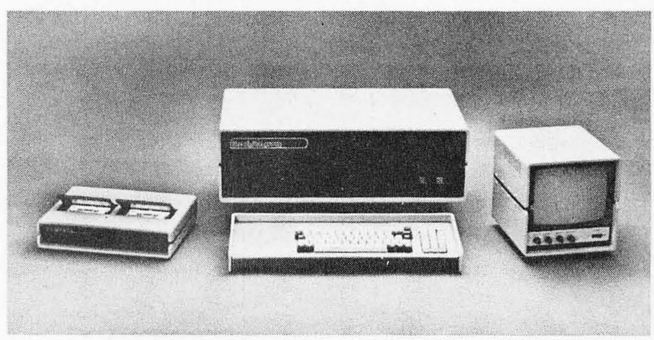
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Madison WI 53706

Jack Breimeir
The Economy Co
1901 N Walnut
POB 25308
Oklahoma City OK 73125

When people first acquire a small computer of traditional design, they are usually content for some time with using the console lights and switches for IO. If the proud new owner has any software aspirations, he or she will soon begin to crave some sort of device to raise the level of intelligence of the man-machine interface. For many, an ASR 33 Teletype or its equivalent makes an ideal first peripheral for a computer system; it gives one a keyboard, a hard copy printer, and paper tape bulk storage for program libraries. There comes a time, however, when the incessant clatter of a 10 character per second paper tape reader is no longer music to one's ears. The fact of the matter seems to be that as the ambition of a programmer grows, so does that programmer's restlessness and impatience to see things being done. There is something irksome about sitting and watching one's IO machine take longer to read a program than it took to code it. The obvious answer is a high speed random access store, like a disk or drum. However, no matter how elegant it might be, not everyone has $5 K for a cartridge disk. Floppy disks are not yet the answer in terms of cost, reliability and media life. Perhaps the best answer for today's amateur may lie with the ubiquitous Philips cassette. There are many alternatives when dealing with cassettes from which to make design choices. Therefore, this article is meant as a reference for ideas, rather than as a construction article.

The theme of this article refers to the use of high performance digital cassettes, so let's define terms. High performance is intended to mean better than the amateur's common forms of automatic program loading, namely Teletypes and low speed audio cassettes. One important performance factor that is easy to improve upon is speed. A Teletype clatters along at 110 bits per second, and an audio cassette at up to 2400 depending on whose system you use, but a digital cassette system begins hitting mechanical limits at 32,000 bits per second (for NRZ1 = 1600 bpi X 20 ips = 32 kbs). A conservatively and therefore more reliably designed system will loaf along at 7,000 to 8,000 bits per second. That's about one thousand characters per second, or 100 times the speed of a Teletype. Imagine a 4 kilobyte program being loaded into main memory in less than 5 seconds. Another, perhaps more important feature possible in an electronically controlled cassette system is a concept known as block replaceability. This means that a block of data on the tape can be erased and overwritten with different data, without disturbing any other preexisting data on the tape. This technique obviously requires very accurate computer control and synchronization of tape motion. Block replaceability is not an easy goal to achieve in the design of a cassette system. In fact, most cassette peripheral system manufacturers do not offer it, and audio cassette drives never have it. Amateurs, however, can do things that professional designers cannot or will not do because amateurs are not as concerned with markets, cost and reliability optimization. Block replaceability is a worthy goal of amateur experimenters in spite of additional hardware requirements because, in conjunction with the proper

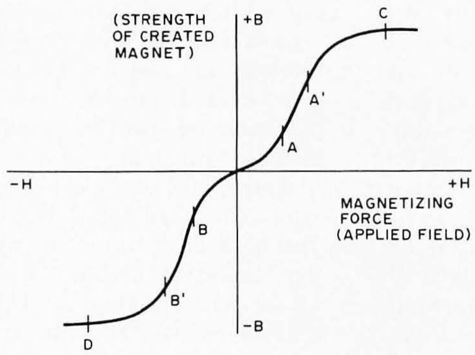


Figure 1: The magnetization curve of the typical magnetic tape medium. The applied magnetic field, H, results in a residual magnet of strength B after the tape has passed the head. The linear regions A to A' and B to B' are used by audio recorders via the trick of using a bias signal which rapidly switches through the A to B region and allows reconstruction of the analog signal intensity based solely on the linear segments. A digital recorder, in contrast, drives the head to saturation (and beyond) at C and D, giving the maximum magnetization possible in either direction.

Part 1, Digital Recording Background and Head Interface Electronics

software device handler, a cassette memory system can simulate a random access device like a disk or DECtape. Although obviously much slower, such a cassette system would enable indigent personal computer users to run the equivalent of a disk operating system, with all of its attendant advantages and features.

Magnetic tape systems of one form or another have been a mainstay of commercially designed computer systems for several decades. As such, there is a fairly large body of information in the engineering literature on the theory and practice of digital magnetic recording. Until now, analog magnetic recording with audio cassettes has been used in the majority of amateur computer applications. A brief look at the physics of analog and digital magnetic recording should convince the reader of the vast superiority of digital techniques.

The fundamental difference between audio and digital recording is in the method and degree of magnetizing the tape. For audio recording, low distortion is a primary requirement. Looking at the B versus H curve (magnetic intensity versus magnetizing force) for tape, figure 1, we see that the curve is mostly nonlinear. Only the linear portions of the curve can be utilized if low distortion is of importance. There are two linear regions from A to A′ and from B to B′ in figure 1. The high frequency bias typical of audio recording is used to insure operation in the two linear regions for the full range of the audio signal level. However, for digital recording as in almost all digital systems, we are interested in only two states: 0 or 1, on or off, true or false or whatever names are convenient for distinguishing two separate states. Two such states are readily available for digital recording, these being points C and D on the B versus H curve of figure 1. Each of these two points is in the saturation region of the curve where a further variation in the magnetizing force results in a negligible variation of magnetic intensity in the tape and both points are in regions of opposite polarity. These then are the two states used for saturated digital recording.

There are several advantages to operating in the saturation regions of the magnetic media which we shall examine now. During readback of magnetic tape, the signal in the magnetic data transfer head is proportional to the rate of change of the flux or

$$e_R = N \frac{d\Phi}{dt}$$

where e_R = instantaneous read head voltage

N = number of windings around head core

$\frac{d\Phi}{dt}$ = change of magnetic flux per unit time

For a given magnetic head and a given tape speed, the maximum readback voltage is obtained by recording a transition of the

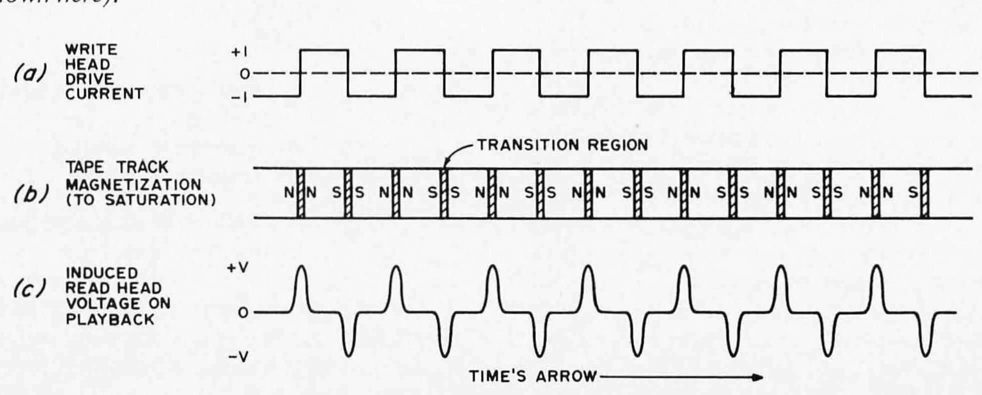
signal from point C to D or D to C of figure 1. In other words, use the maximum possible change of flux in order to take advantage of the full amplitude capability of the magnetic media. This results in the maximum readback signal which in turn gives the highest signal to noise ratio. Secondly, since the tape is being saturated there are no critical bias levels or record current levels to maintain. All that is required is that the current through the record head be of sufficient value to operate at or above the knee of the B versus H curve. Most digital systems operate at record head current levels of 125% tape saturation or above. Because this level is well above saturation, the exact value is not critical and, therefore, no adjustments are required in the recording electronics during manufacture or during maintenance.

As previously mentioned, the manner in which the signal is used to designate ones and zeros for digital systems is different from the techniques used for audio. In audio the high frequency bias switches between the two linear regions of the tape while the audio is superimposed on the bias for recording the information. When audio recording techniques such as frequency shift keying (FSK) are used for storing digital information, typically 4 to 8 cycles of an audio tone are recorded in combination with the 50 to 100 kHz high frequency bias. During readback, the audio tones are recovered and converted back to digital information. Saturated digital recording systems require no such complication. Each excursion from one saturation polarity to the opposite is of significance. These magnetic polarity reversals are called flux transitions or flux reversals and, generally, less than one to a maximum of two are required per bit of digital information.

Let us now take a closer look at what the saturated digital signal looks like on tape. The head drive current is switched between the saturation currents as shown by the square wave in figure 2a. The result is that cells of magnetization are recorded on the tape as shown in figure 2b. The magnetic cells alternate in polarity corresponding to the direction of the recording current. When the tape is read back, the read head will have a voltage induced only at the cell boundaries where there is a large change of flux. The resulting input head waveform is shown in figure 2c. Notice that the head has an output only at the locations where the flux changes occur and no output between flux changes where the remanence magnetism is constant. The magnetic head output when reading is obviously much different than the recorded current waveform. This situation is quite the opposite of the requirements for audio systems where the playback voltage must be a faithful reproduction of the record current.

Another difference between audio and digital recording worth noting is in the method of erasing tape. Audio tape must be erased with a high frequency signal to replace the recorded signal with a completely random jumble of magnetic cells, or domains, that produce no signal. If this prior erasing is not done, then the new audio signal is simply added to the previously recorded signal, achieving a "sound on sound" effect. Saturated digital recording eliminates the need for an erase head, and a separate erase process. Since saturated recording forces the tape to comply completely with the new data, the previous state of tape is irrelevant. Digital recording erases

Figure 2: Timing and tape positioning in a digital recording. At (a) is shown an example of a square wave applied to some tape head, alternating between two saturation current levels arbitrarily called +1 and −1. The result is a pattern of magnetized regions on the tape, with boundaries at each transition point. The passage of the magnets over the head during a read operation induces a current pulse proportional to the rate of change of the magnetic field's direction. Here we've arbitrarily given NS as the designation for a +1 current state, and SN as the designation of the −1 current state at write time. The trace at (c) shows the voltage integral of currents due to the field transitions of (b) when the tape is read. The key to recording digital data is the creation of a time format for the transitions of the fields (which don't have to have the regular pattern shown here).



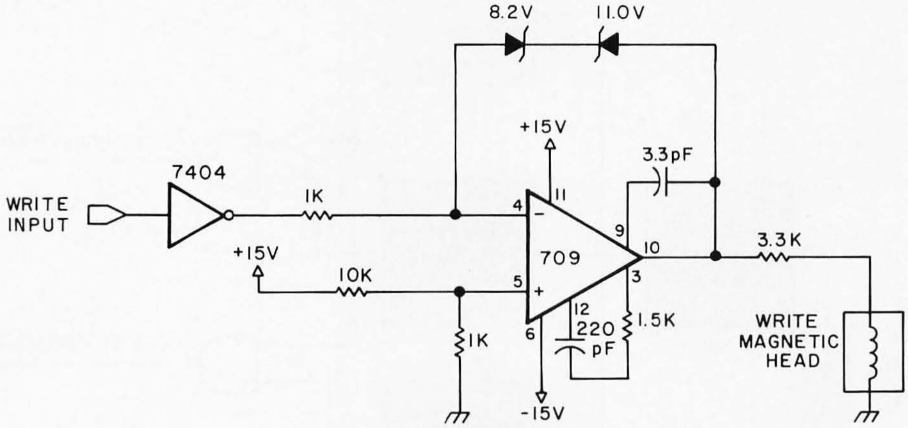


Figure 3: A typical head drive circuit for saturation recording. The 709 operational amplifier here is used to drive the magnetic tape head to saturation in either direction by applying a 10 V signal with respect to ground. A magnetic recording head winding resistance of typically 100 ohms in the digital cassette case results in a current of 10/3400=0.003 A (3 mA).

the old data automatically with every write. Some digital recorders do have an erase head, usually called a tunnel erase head. These erase heads are only used to insure compatibility between different decks. Because different decks have different mechanical head to tape relationships, the tunnel erase heads erase a track much wider than the head records on. This wide swath of erasure insures data recorded on a different machine can be erased completely, in spite of a slight head misalignment. The convention when purposefully recording a blank piece of digital tape is to simply saturate the head in one direction for the entire blank section.

In digital systems, the data or information is determined by these flux transitions rather than by any continuously varying analog signal. There are many different combinations in which the transitions can be used to designate a 1 or 0. The polarity, position, or relative spacing of the transitions are all possibilities. The process of assigning information to the flux transitions and recovering it is termed encoding and decoding. The more popular methods of encoding and decoding are covered later in this article.

Recording or writing flux transitions onto tape is relatively straightforward. Digital cassette magnetic heads typically require 4 to 10 mA peak to peak current for saturation of the tape. This amount of current drive is easily available from a general purpose operational amplifier. Figure 3 is a circuit diagram of a typical write amplifier that delivers plus and minus 3 mA current drive to the magnetic head. The circuit consists of a 709 operational amplifier with back to back zener diodes providing bipolar limiting. TTL logic level inputs are applied to the write data input, inverted and then supplied to the inverting input of the op amp. The noninverting input of the op amp is referenced at 1.4 V positive, thus the output will switch polarities when the input changes from one TTL level to the opposite.

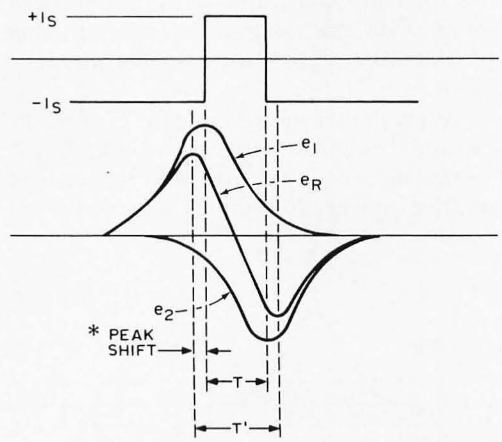


Figure 4: Merging of transitions. When two transitions come close together on the tape, the response curves (see figure 2c) upon reading the data can overlap significantly. This crowding of flux changes tends to cause interference such that the amplitude of the signal is reduced, and the time coordinate of the peak of the curves will shift slightly.

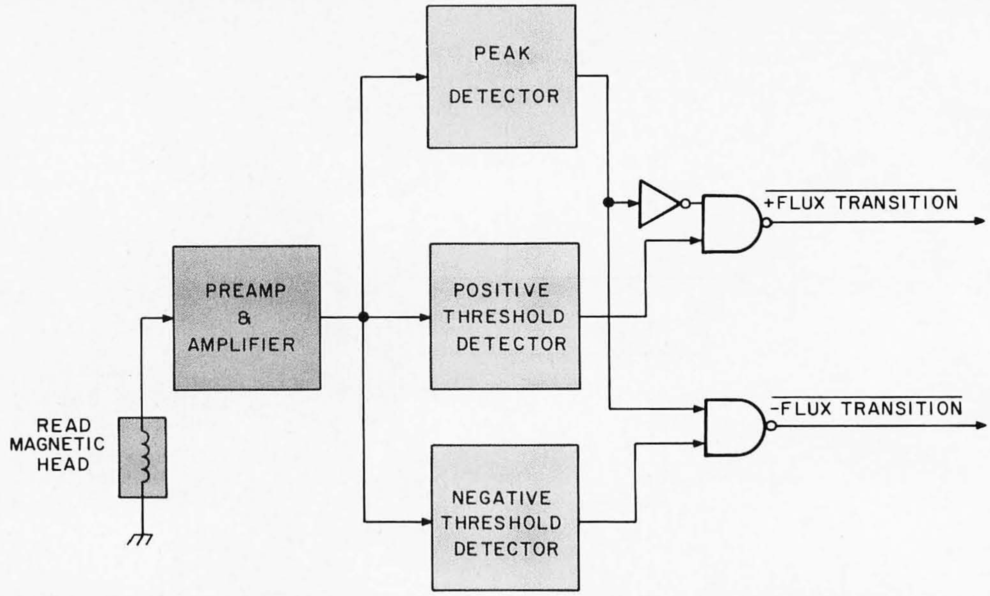
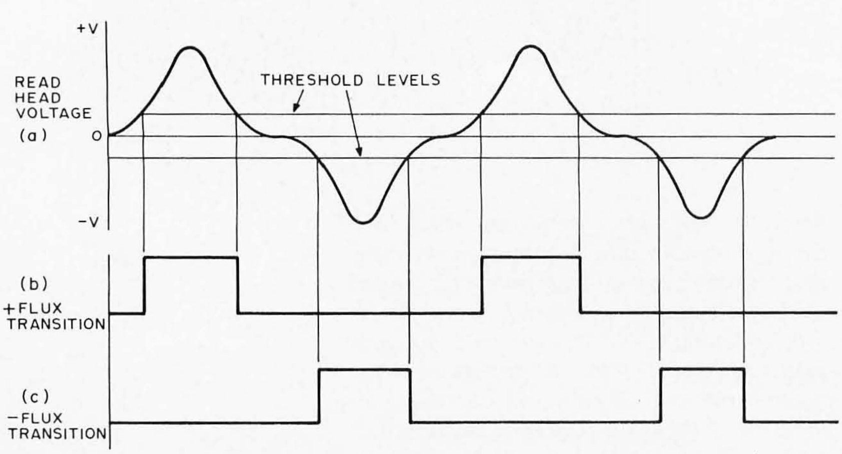


Figure 5: Block diagram of typical magnetic tape head read electronics for digital recording. The preamplifier and amplifier sections merely turn the very weak signal actually generated in the head during a read data transfer into a strong enough signal to analyze. The peak detector marks the time at which the peak negative or positive amplitude is achieved, and the positive or negative threshold detectors merely gate the direction in which the signal was detected. The result is a pair of lines, one having a pulse for each + transition, one having a pulse for each − transition.

Figure 6: Time relationships of the voltage waveform from the head (a), the positive threshold detector output (b), and the negative threshold detector output (c). The threshold outputs serve as a gate for the peak detector. (Refer to figure 5 for the system block diagram.)



The output is clipped at plus and minus 10 V by the negative feedback through the zener diodes. Since the inputs to the op amp are offset 1.4 V above ground, the zener diodes are 8.2 and 11.0 V units to provide a symmetrical ±10 V output. The resistance of a cassette digital magnetic head is typically less than 100 ohms, thus, a 3.3 k resistor in series with the output of the op amp provides the ±3 mA drive to the magnetic head.

As previously shown in figure 2, when the recorded magnetic pattern is read back, the voltage induced in the read head is a series of positive and negative pulses occurring when the flux transitions cross the head gap. The flux transitions have been shown widely spaced with no interaction. In order to achieve maximum storage density and highest data transfer rates, the flux transitions are normally written close together. When this is done, the interaction between transitions must be taken into account. Because of the physics of the magnetic tape to tape head system, flux transitions recorded on tape are not infinitely narrow. The resulting induced readback voltage is a pulse shaped somewhat like half a sine wave. When two closely spaced transitions are read, the results are as illustrated in figure 4. I_S is the recorded saturation current; e_1 and e_2 are the induced read voltages which would occur if the transitions were widely spaced; and e_R is the actual resultant read voltage due to the close spacing of the transitions. The trailing and leading edges of one pulse overlap into the areas occupied by adjacent pulses. The result is a reduction in amplitude of each pulse. This phenomenon is called pulse crowding. A close look also reveals a shift in the position of the peak of the pulse. This is known as peak shift.

Another consideration in magnetic tape is the amount of *dropout* allowed. Dropout is a momentary decrease or loss of signal amplitude during readback, due to minor imperfections in the tape magnetic material

or tape to head interface. Digital grade cassettes are certified to have no more than 50% loss of amplitude of a signal recorded at 1600 flux reversals per inch (FRPI). Audio grade cassettes generally are not certified and it is up to the manufacturer's discretion as to the amount of dropout permitted in his product.

What the preceding two paragraphs mean in terms of digital tape signals is that, instead of constant amplitude readback signal, there will always be random amplitude variations in the signal and shifting of the pulse peaks depending on the flux transition pattern written. The pulse crowding peak shift and dropout rate limit the maximum flux density that can be utilized for digital tape if error free data storage is a requirement. The maximum flux density for cassette tape is normally 1600 FRPI. In addition, the design of the read amplifier is a key element in minimizing the effects of the above tape characteristics.

Figure 5 is a block diagram of a typical read amplifier. The signal from the magnetic head is amplified in two stages by a low noise preamplifier and amplifier. The analog signal at the output of this block is about 4 V peak to peak. The signal is then applied to the peak detector and plus and minus threshold detector. The threshold detectors accept analog signals as inputs and have logic level outputs. When the input signal is below a preset reference level, the output of the positive threshold detector is a logic low. When the analog signal at the input exceeds the positive reference or threshold value, the output is a logic high. The negative threshold detector operates in the same manner except that it detects negative pulses. These signal relationships are illustrated in figure 6. The threshold detectors effectively isolate the low level noise and the amplitude variations from the read signal while supplying logic level pulses as an output for further processing.

Even though the threshold detectors remove amplitude variations from the read signal, there will be time jitter in the outputs due to these variations as illustrated in figure 7. This effect can be eliminated by detecting the peak of the analog read signal, then combining the result with the threshold information. This is the function of the peak detector block in figure 5. The sequence of events and resulting outputs is shown in figure 8. Note that we now have logic level information that accurately locates the center of the flux transition at a logic signal edge with no timing or amplitude variations due to amplitude fluctuations in the read signal.

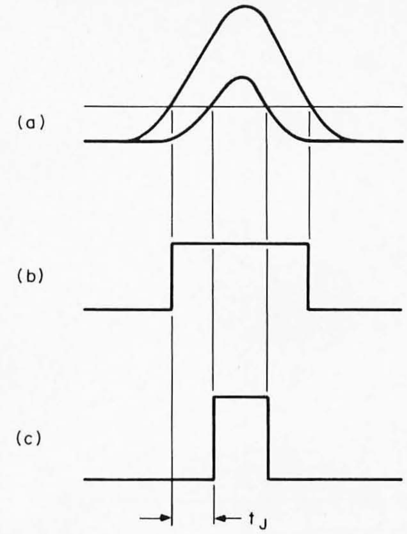


Figure 7: A superimposition of a strong signal and a weak signal (a) shows how there can be considerable jitter in the threshold detector outputs. At (b), the strong signal quickly reaches the threshold when it is rising, and remains above the threshold for a longer time, thus resulting in a wider pulse than at (c) where the lower amplitude signal is read. In the normal operation of the tape, crowding effects such as seen in figure 4 and the dropout effect together require that the input circuitry be tolerant of amplitude variations.

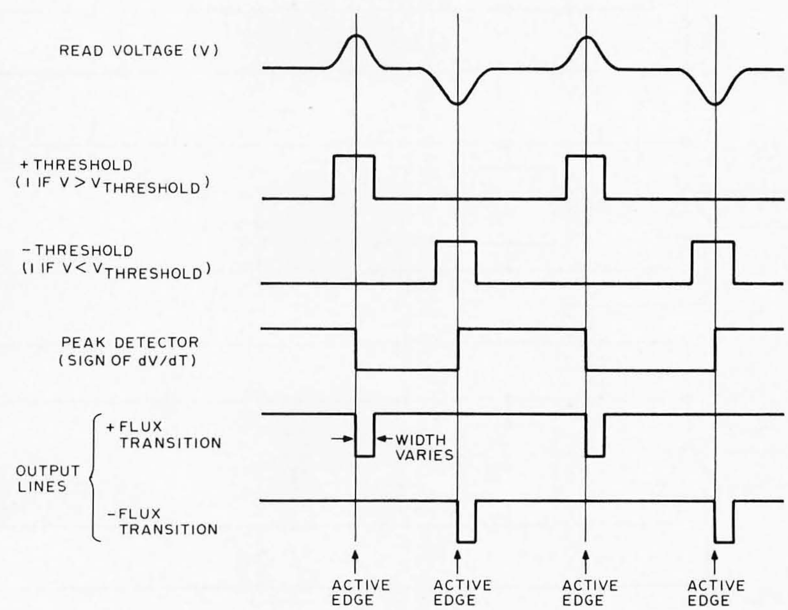


Figure 8: Decoding begins using a peak detector, which changes its logic state at the time the derivative of the voltage with respect to time changes sign. The peak detector output is then gated with the threshold detectors resulting in a pulse which has a negative transition at the peak, and a width dependent upon the amplitude of the signal. The negative edge of the flux transition lines is the derived clock reference used for input operations.

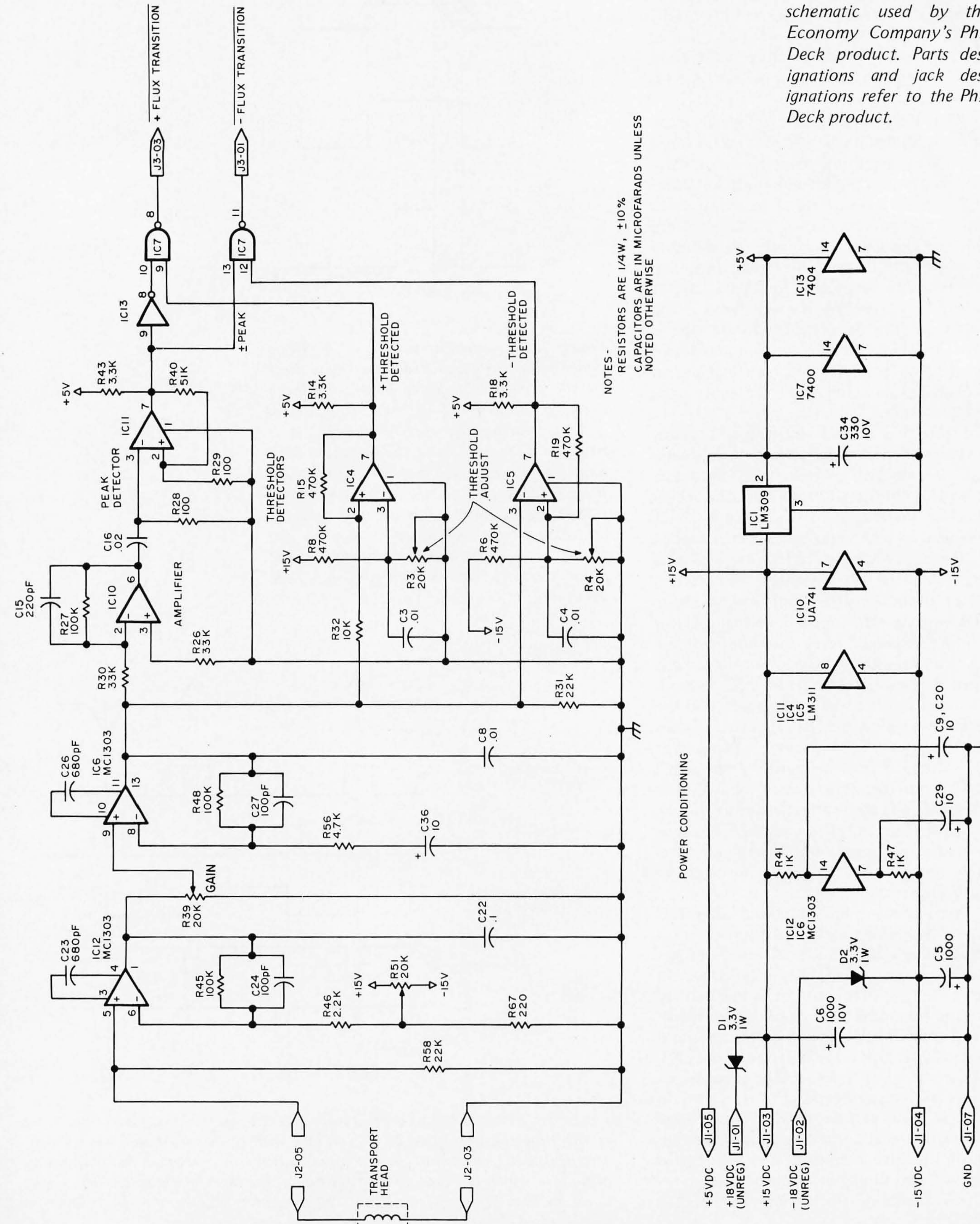


Figure 9: Details of a digital recording read head signal processor. This circuit is drawn from the schematic used by the Economy Company's Phi-Deck product. Parts designations and jack designations refer to the Phi-Deck product.

Let's take a look at some of the detail circuitry of a read amplifier. Figure 9 is a schematic diagram of a read amplifier corresponding to the block diagram of figure 5. The preamplifier and amplifier consist of a MC 1303 dual, low noise audio amplifier. The amplifier circuits are a standard op amp configuration with negative feedback controlling gain and frequency response. The feedback elements for the first stage consist of R45, R46 and C24. Midband gain is set by R45 and R46. The high frequency 3 db corner frequency is determined by R45 and C24. R51 is an offset adjustment to provide for zero offset voltage and R39 is a gain adjustment for the signal level. The second stage is similar to the first with the addition of low frequency rolloff determined by R56 and C36. The two stages combined have an overall gain of approximately 1000 with 12 db per octave rolloff above the upper cutoff frequency and 6 db per octave below the lower cutoff frequency. Different encoding and decoding methods have different read amplifier bandpass requirements. The read amplifier gain and bandpass requirements are also dependent upon the tape speed. The read amplifier bandpass should be tailored to pass only the frequencies required by the system; thus, the highest signal to noise ratio is obtained.

The threshold detectors consist of LM311 comparators, IC4 for positive pulses and IC5 for negative pulses. One input of each of the comparators is connected to an adjustable reference voltage. The reference voltages can be varied to select the level or threshold value at which a pulse is considered a valid flux transition. Resistors R15 and R19 supply negative feedback to give a small amount of hysteresis. This prevents the comparator outputs from oscillating during switching. By grounding pin 1 of the comparator and returning the output to +5 V through a pullup resistor, the outputs are TTL logic levels.

The peak detector consists of an amplifier stage, IC10; a passive differentiator, C16 and R28; and a zero crossing detector, IC11. The amplifier provides gain to compensate for the attenuation of the differentiator network. The output of the differentiator will be a positive or negative voltage corresponding to whether the analog signal has a positive or negative slope. The differentiator output is supplied to the zero crossing detector, IC11. The output of IC11 will be a high or low logic level changing states only when the differentiator output changes polarity, thus locating the peak of the readback pulse.■

Next month cassette decks, encoding schemes, and applications will be discussed.

Ask BYTE

Some letters to BYTE are technical in nature and are best served by some form of response. We will try to answer as many such letters as possible. If you have a puzzle concerning some aspect of the personal computing field, write down a clear statement of your question and send it to:

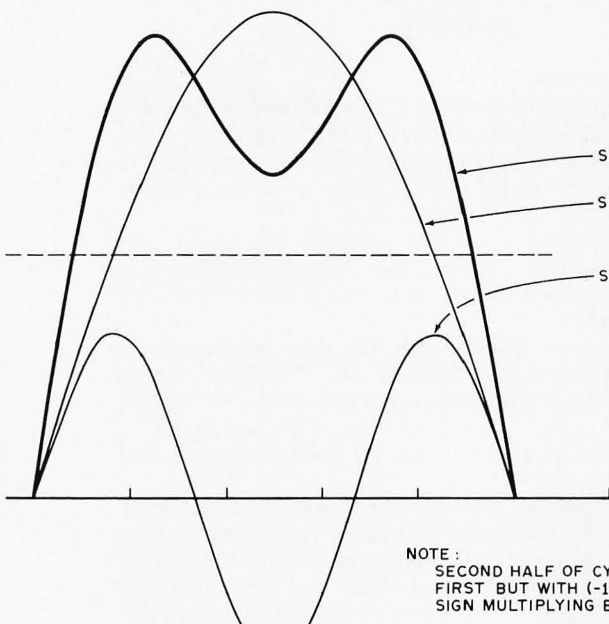
Ask BYTE
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We will publish names and addresses of individuals making inquiries unless you specifically request us to omit the reference.■

Got my first issue of BYTE yesterday and was much impressed by content and format. I was especially interested by Dr Suding's article on a TV interface *[August 1976, page 66]* since I'd like a demand terminal to our U1108 computer. It needs 80 char/line, so his bandwidth comments grabbed my attention to say the least.

In the hope that I didn't really understand what he said, could we review? With 8 bits/char (7 in the matrix + 1 space) and 32 chars/line it looks like you have 256 bits/line. At standard deflection rates, yielding 53.34 µs trace time, that works out to about 4.8 Mbits/second. Since the worst case pattern is alternate ones and zeros, it looks like bandwidth for the fundamental frequency must be at least 2.4 MHz. Did I miscalculate or do you really need to pass the third harmonic?

Steve



*[***Note:*** This letter was received from a person who signed it "Steve" with no return address; as sometimes happens, the envelope was discarded before the discovery that there was no return address or other identification on the letter itself. This problem of identification is the reason for requesting our authors to record their names redundantly in packages sent to BYTE.]*

*First, note that with a 256 bit pattern of alternating light and dark, the worst case for bandwidth purposes, the actual frequency of the video data is found by dividing 128 (a two segment pattern is involved) into 53.34 µs, not 256. Thus the frequency of the fundamental in the 256 element display is 2.4 MHz worst case (417 ns per 2 bits). In order to make a passable (first) square wave appoximation, Fourier analysis from an elementary mathematics course shows that the first two terms are the fundamental and the third harmonic, in a ratio of 1 to 1/3 in amplitude. Thus the amplifiers for a first order representation of a digital signal on the scan line should be able to pass 2.4 * 3 = 7.2 MHz if no distortion of the first order approximation is to occur; in fact somewhat less than a flat response will still allow an image to be seen and understood, as is demonstrated by the fact that TV displays on standard sets work at all. The results of low bandwidth are a smearing together of the picture elements.*

The same considerations apply when thinking about the typical commercial display monitor with its nominal (flat) response bandwidth extending in the 15 to 25 MHz range. Take the example of an 80 character display with 8 picture elements per character. The number of picture elements per scan line is then 640; and keeping the same scan time, this gives 83.33 ns per picture element. In the worst case alternate state display, two elements, or 166.7 ns, are required for each cycle, giving a frequency of 5.99 MHz. The third harmonic of this frequency is 17.97 MHz. Thus on a monitor with 15 MHz nominal bandwidth there might be some smearing or loss of definition due to less than unity gain for the third harmonic, and on monitors with higher bandwidth, a sharper picture would be obtained. For reference, accompanying this note is a picture of the third harmonic approximation to a square wave and the first and third harmonic terms in isolation.■

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Build This Economy Floppy Disk Interface

Dr Kenneth B Welles
General Electric, Nela Park
2623 Fenwick Rd
University Heights OH 44118

The floppy disk drive offers the advanced computer hobbyist tremendous potential for a high performance computer system. With one or more floppy disk drives, an interface, and the proper operating software, the hobbyist can store hundreds of different programs on a single disk. Each of the programs can be given a name such as STARTREK, BASIC or EDIT, and a program can be run simply by typing its name, for instance "RUN EDIT". With this interface, the program can be brought into the computer at speeds of up to 31,250 bytes per second (for programs less than 5000 bytes long in the proper format). Each disk will store over 300,000 bytes of programs, computer music, Dazzler graphics, ASCII text, synthesized speech thesaurus or data of any form, and any data on the disk can be accessed in at most one second, typically in less than one quarter second. In fact, the draft of this article was written and edited using mass storage on a disk drive in my personal home computer system. The entire article takes up less than seven percent of one floppy disk, and the time saved in the retyping of successive revisions of the article was tremendous. *[Groan! Do I wish I had a floppy disk, CRT display, HYPERTEXT software and input scanners in my office . . .* CH]

Floppy disks also allow the quick assembly of large programs, without having to start, stop and rewind cassette players. Proper software allows a single floppy disk drive to merge several data files into one ordered file (for the updating of mailing lists or financial records), an operation which would take several cassette recorders on a cassette based operating system.

All of the features mentioned are the potentials of a floppy disk computer system. For a personal computing user to realize these potentials, he or she needs both

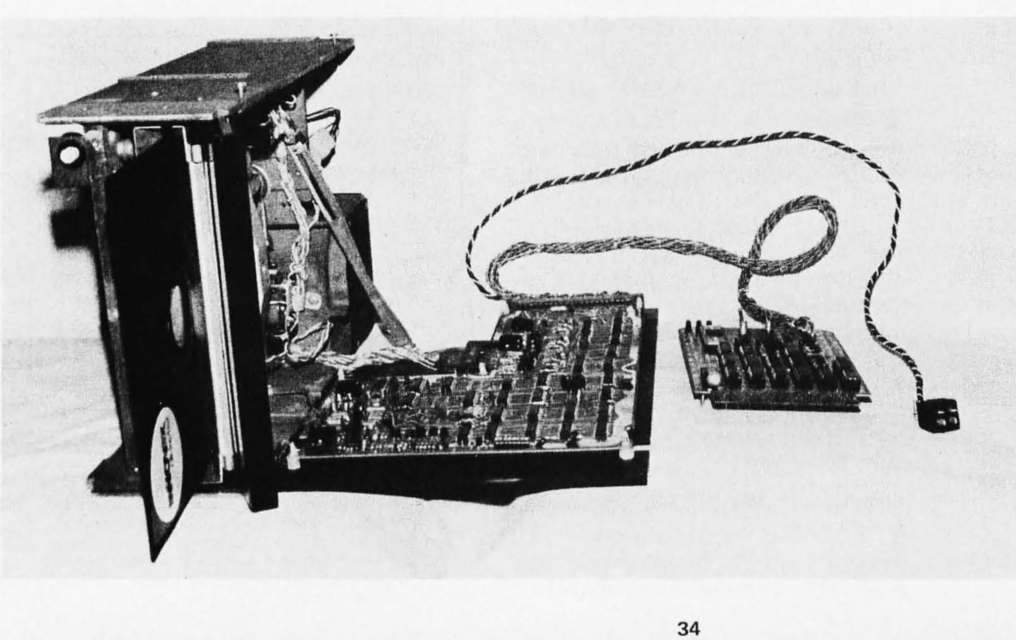


Photo 1: The author's disk drive and interface board shown removed from the system. The Innovex drive is at left, with a diskette partially inserted in the front door and the electronics board for the drive shown in an "open" position. The interface board is at the end of a multiconductor twisted pair cable, and a separate cable is used for drive power.

About the Author

Dr Welles is an enthusiastic personal computing user, with a fairly well developed system. At the time he wrote the current article, his system included an Altair processor, 14 K programmable memory, 5 K of 2708 ROM, and 2 Innovex floppy drives interfaced to the system. Miscellaneous peripherals include homebrew versions of a paper tape reader, television display, a modified office Selectric typewriter output, vector graphics, television camera input, and TV dazzler outputs among others. His main interests are image processing, pattern recognition, computer graphics and robotics. The entire text of his draft was typed and edited on his system, with hard copy output printed on the Selectric as the draft text submitted to BYTE. [At some yet to be determined future date, we'll eliminate the paper step and have authors such as Dr Welles simply send an appropriate machine readable representation of their articles . . . **CH**]

hardware and software. This article covers a hardware interface for floppy disk drive units.

Until recently, only the well financed hobbyist could afford a floppy disk drive for a personal system. In addition to the $650 to $1000 cost of the drive unit, one was also forced to spend from $300 to $1500 for a floppy disk drive controller. The high price of the controller buys a very intelligent electronic device, however. A single command from the computer causes the controller to seek a particular track on one of up to four disk drive units, load the head, find the desired sector, format and read or write the data, calculate the CRC (Cyclic Redundancy Check), determine if the transfer had been successful, and retry the transfer in the event of a read or write error. The design of such an intelligent controller is based on the old school, IBM/360 approach that processor time is too valuable to waste doing the housekeeping for a peripheral device. A personal computing user, on the other hand, has lots of processor time, limited funds, and consequently a different philosophy. One of the original reasons for the development of microprocessors was to perform in software all of those functions that would normally (and expensively) have to be designed in hardware. In this vein, in collaboration with W R Hemsath of Cornell University, I have designed and built a floppy disk drive interface which incorporates minimal hardware, and yet does not sacrifice the flexibility needed to read and write various data formats. This interface consists of only 17 integrated circuits, only one of which is a special purpose chip. The total cost of the chips is less than $25. The design shown here will interface up to eight floppy disk drives to an 8080 processor. In order to properly describe the design and function of the interface, let us first review briefly what steps are required to transfer data to or from a floppy disk.

Disk Drive Operation

In operation, a disk is inserted into the drive and the access door is closed. The act of closing the door engages the disk onto the spindle, and the disk is then rotated at 360 RPM. A stepper motor drives the magnetic data transfer head radially in and out to 77 discrete positions, the outermost called track 0 and the one nearest the center of the disk called track 76. Normally, the head does not touch the spinning disk, but is positioned a small distance away from it. When data is to be read or written, a modified relay is energized allowing a spring loaded pressure pad to press the flexible disk into contact with the head. Timing holes punched in the floppy disk pass by a photo detector and generate a series of pulses. These "sector pulses" are used to determine which one of 32 segments or sectors of the disk is currently passing the head. Use of such holes to define sectors is called "hard sectoring" in disk drive jargon. The pulses are used to signal the approximate starting point of each sector. Data is read from and written to the disk in a manner quite similar to the reading and writing of data on magnetic cassettes. In normal operation, each of these 32 sectors will store slightly over 1024 data bits, or 128 bytes. To write data onto a particular track and sector of the disk, the following operations must take place:

1. The head is moved in or out to the desired track.
2. The pressure pad is loaded, pressing the disk against the head.

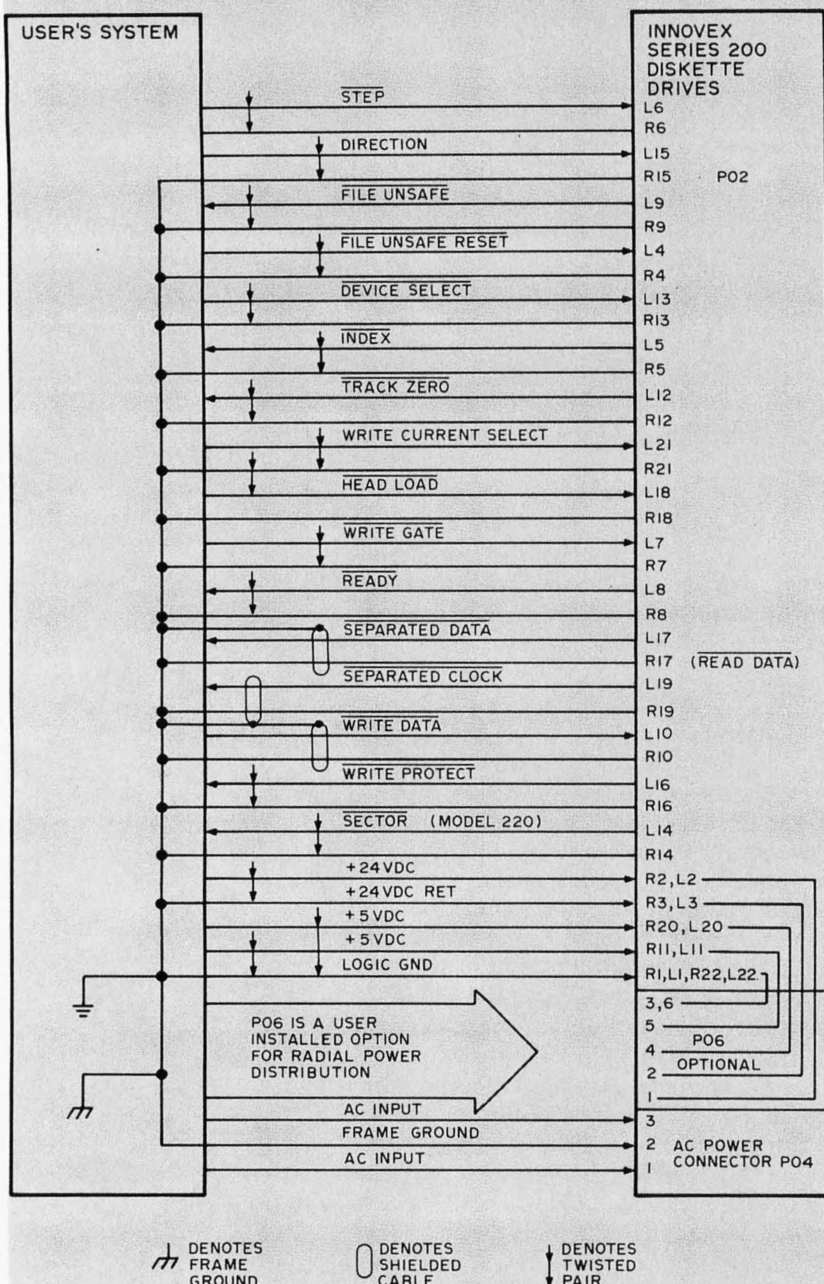


Figure 1: This diagram, redrawn from the Innovex Series 200-M Maintenance Manual, *shows all of the TTL level signal lines that must be passed between the disk drive and the controlling interface.*

The signals sent to the drive from the interface are:

Device Select: When this line is high, all commands from the interface are ignored by the drive, and all signals from this drive unit are put into a high impedance state. If several drives are used, all of the input and output signals may be tied together on a common bus with the exception of the device select lines. By pulling only one of the several device select lines low, the interface selects that particular disk drive to send commands to and receive data from.

Step: A low going pulse on this line causes the head positioning motor to move the data transfer head in or out one track.

Direction: During a step pulse, if this line is high then the head moves out one track (towards track 0). If this line is low, then the head will move in one track.

Head Load: When this line is low, the pressure pad brings the spinning disk in contact with the data transfer head.

Write Current Select: Because the surface velocity of the disk relative to the head varies from the outermost to the innermost track, the density of the data on the disk will also vary. To compensate for this variation, the write current select line varies the amount of current used to write data as a function of the track being written. This line must be low when writing data onto tracks 0 to 43, and high for tracks 44 to 76.

Write Gate: Pulling this line low enables the data on the write data line to be sent to the head and recorded onto the disk.

Write Data: Data to be written on the disk must be serialized and sent out on the write data line as a series of low going clock pulses (one pulse every 4 μs) separating the presence (a 1 data bit) or absence (a 0 data bit) of a low going data pulse. Figure 2 shows the write data signal used to send the data bit string 10100 .

File Unsafe Reset: This line is pulsed low just before a write operation is to take place. The pulse resets the file unsafe status to a safe (write enabled) condition, thereby allowing the write operation to be performed.

The signals sent to the interface by the disk drive are:

File Unsafe: A low signal on this line indicates that an error condition existed when a write operation was attempted. When file unsafe goes low, no writing can be done on the disk, preventing the loss of previously written data due to some error condition.

Track Zero: When the data transfer head is positioned at track 0, this line goes low, enabling the computer to calibrate the head position. When the head is at tracks 1 to 76, this line is high.

Index: A 500 μs low going pulse appears on this line to signify that the index hole has just come into position under the photodetector. This pulse is used by the computer to determine which sector is sector 0.

Sector: A 500 μs low going pulse appears on this line each time a sector hole (not an index hole) passes under the photodetector. 32 pulses occur every revolution, and these pulses are used to determine the approximate starting positions of the various data sectors.

Ready: When AC and logic power are present at the disk drive and a disk is loaded, the ready line goes low.

Separated Clock: When previously written data is being read from the disk, the clock is recovered from the data stream, and is presented on this line as a series of 200 ns low going pulses. The recovered clock pulses come approximately every 4 μs with variations due to the changes in drive motor speed.

Separated Data: The serial data coming from the disk during a read is indicated by the presence (a 1 data bit) or absence (a 0 data bit) of a 200 ns low going pulse on the separated data line, between adjacent separated clock pulses.

Write Protect is an optional signal that is not used in this interface. On a disk drive with this option added, the user can write protect the data on a disk by punching out or uncovering a write protect hole in the disk jacket. A write protected disk cannot be written onto.

3. Sufficient settling time is allowed for the head movement and pressure pad loading to fully stabilize.
4. Delay until the start of the sector pulse which corresponds to the desired sector.
5. Turn on the WRITE GATE of the disk drive to allow data to be written.
6. Write 64 0 bits (16 bytes of 0).
7. Write a single synchronizing byte (sync byte).
8. Write the desired data bytes.
9. Write 64 0 bits.
10. Turn off the WRITE GATE to prevent any more data from being written.
11. Unload the pressure pad.

Because the disk drive records data serially, steps 7 and 8 require that each byte being written must be sent out as a series of 8 bits, with one bit being sent out every 4 μs, and with no skipped bits between bytes.

Reading data from the disk requires a similar series of operations:

1. The head is moved to the desired track.
2. The pressure pad is loaded.
3. Settling time is allowed for movement and loading.
4. Wait for the start of the sector pulse corresponding to the desired sector.
5. Search for the first occurrence of the sync byte.
6. Read in the desired data.
7. Unload the pressure pad.

Searching for the sync byte entails shifting the incoming serial data into a 8 bit byte and comparing the result of each shift with what the sync byte should be, every time that a new bit is read (every 4 μs). When a match is found, then the data bit stream that follows is broken into bytes on every eighth bit, using the sync byte boundary to define the data byte boundaries that come after the sync byte.

From the proceeding lists of read and write procedures, two things become apparent: First, the speed required for shifting data in and out (1 bit every 4 μs) is too fast for most microprocessors to handle under software control (and searching for the sync byte is more time consuming still!). Second, all of the other operations (stepping the head from track to track, loading the head, searching for the proper sector pulse and turning the write gate on and off) are easily within the capabilities of microprocessor software control. Therefore a minimum hardware interface should control all of the functions which are not time-critical, through software and a simple input and

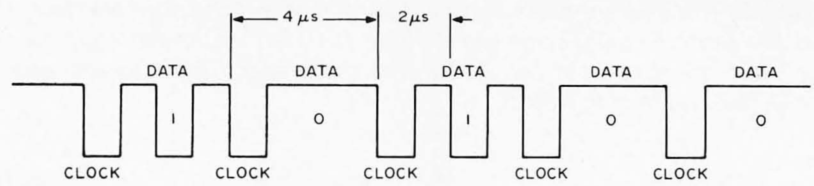


Figure 2: The timing of data cells on the disk. Each bit cell is framed by a clock pulse on either side. If the data is 1, a pulse appears in the middle of the 4 µs cell width; if the data is 0, no pulse appears in the middle of the cell. The waveform in this example has 5 cells with the pattern of data needed for the string 10100.

latched output port. The remaining functions then determine the major portion of the design.

The disk drive we used for this interface is an Innovex 220 hard sectored flexible disk drive, and the signal lines required to operate the drive are typical of most floppy disk drives. There are 15 standard TTL level signals required to operate the model 220 drive, 8 from the interface to the drive, and 7 from the drive to the interface. The signal names and functions for the interface are summarized in figure 1.

Figures 3 and 4 show the circuitry of the floppy disk interface. The circuit has 6 major sections: processor IO instruction decode, instruction latch to disk drive, status load from disk drive, head load-unload, USRT transmit, and USRT receive.

Table 1: Semantics of the OUT 243 instruction. This table lists each accumulator bit, along with its meaning when used to transfer data to the disk interface in the OUT 243 instruction of an 8080. (In a different wiring of the IO instruction decoder, or in a different computer, the same format could be used for the actual data transfer.)

OUT 243 INSTRUCTION

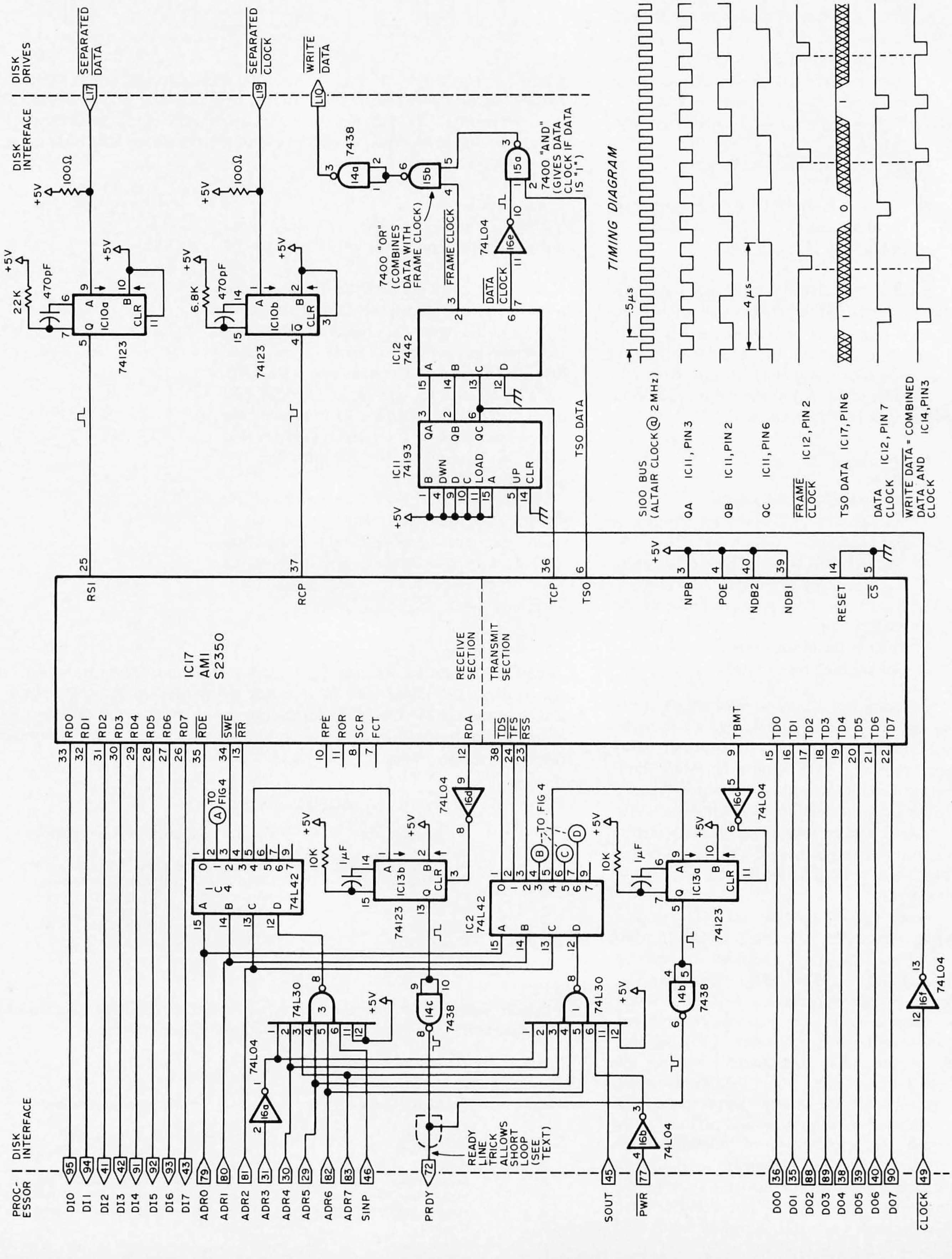
Bit	Signal Name	Polarity in Accumulator
0	Write Current Select	1 for tracks 0 to 43, 0 for track 44 to 76
1	File Unsafe Reset	0 to 1 to 0 transition causes reset
2	Direction	1 for step in, 0 for step out
3	Write Gate	1 enables the drive to write
4	Step Track	0 to 1 to 0 transition steps one track
5,6,7	Drive Select	000 selects drive 0, 111 for drive 7

Table 2: Semantics of the IN 241 instruction. This table lists the status bits read by the IN 241 instruction of an 8080 using this interface.

IN 241 INSTRUCTION

Bit	Signal Name	Polarity in Accumulator
0	Track Zero	0 means the head is at track 0
1	File Unsafe	0 means file unsafe condition exists
2	Ready	0 means disk drive is ready
3	Sector Hole	1 to 0 transition marks start of each sector
4	Index Hole	0 means that the next sector is sector 0
5	Head Loaded	1 means that the head is still loaded
6,7	Unused	Always 1

Figure 3: This diagram shows the major portion of the disk drive interface. IC1 and IC2 form the output command decoder. IC3 and IC4 form the input command decoder. IC10 sets up the data from the disk into a format acceptable to the USRT. IC11 and IC12 put the data from the USRT into the proper format for the disk drive. A list of all integrated circuits with power connections is found in table 3.



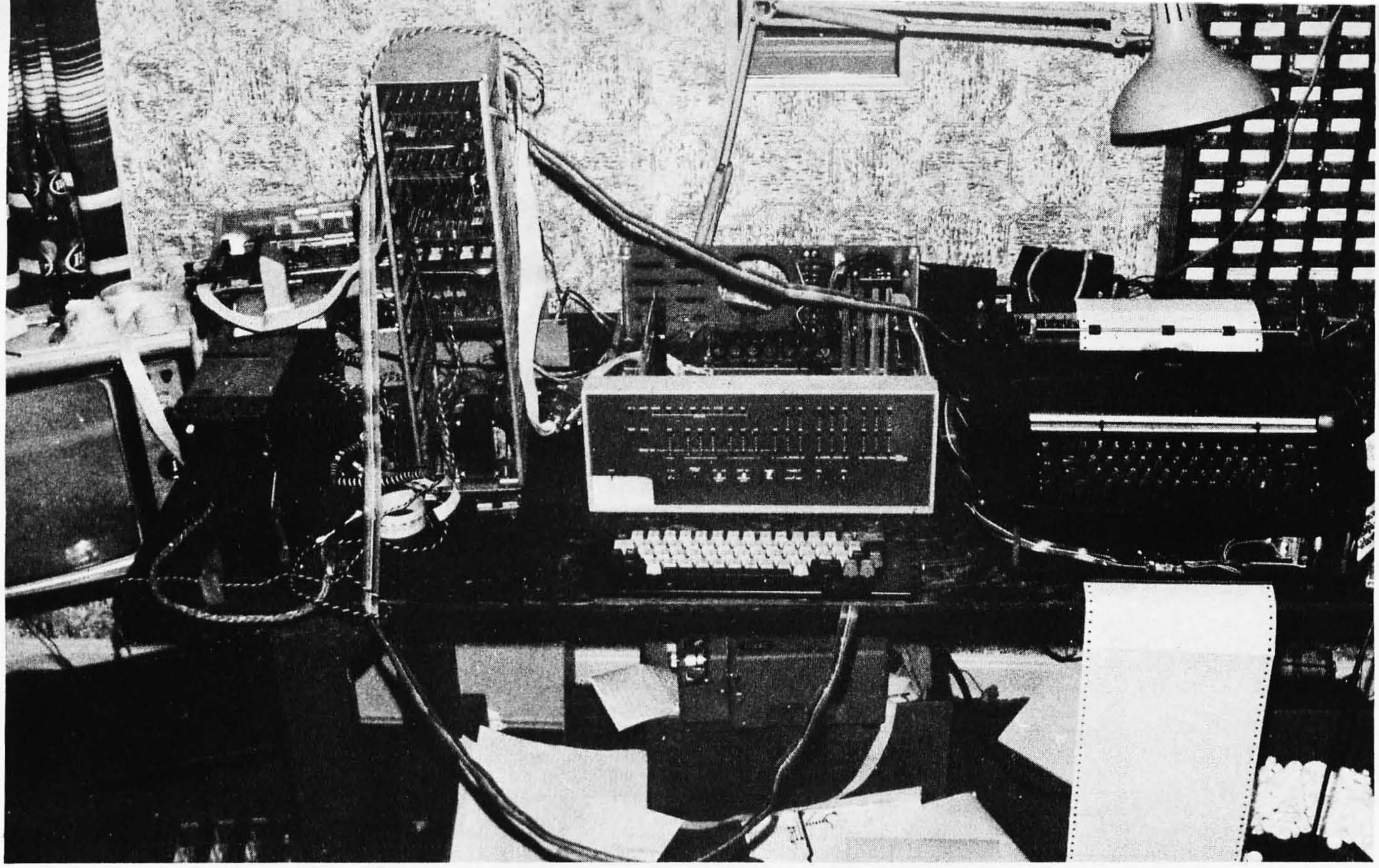


Photo 2: The author's system. The processor is an Altair, and other peripherals include a homebrew Selectric typewriter interface . . . .

Processor IO Instruction Decode

IC1 and IC2 decode output instructions to the interface. Executing the 8080 instructions OUT 240, OUT 241, . . . OUT 247 (240 to 247 decimal) cause 500 ns low pulses on the output lines 0 to 7 of IC2. These pulses can be used to latch data from the output data bus lines DO0 to DO7 into various registers, or to trigger specific functions (as will be shown later).

IC3 and IC4 form the input instruction decoder for the instructions IN 240 to IN 247 in a similar manner to the output decoder. The pulses on the output lines of IC4 are used to gate data onto the input data bus lines DI0 to DI7 and into the accumulator. Again, the pulses may be used to trigger specific functions that are not data input operations. *[In adapting this design to a non 8080 based computer, this decoding logic would have to be modified . . . .* CH]

Table 3: Integrated circuit power wiring list. This table lists each integrated circuit in the floppy disk interface, along with its power wiring pins.

Number	Type	+5 V	GND
IC1	74L30	14	7
IC2	74L42	16	8
IC3	74L30	14	7
IC4	74L42	14	7
IC5	74LS175	16	8
IC6	74LS175	16	8
IC7	7442	16	8
IC8	8097	16	8
IC9	74123	16	8
IC10	74123	16	8
IC11	74193	16	8
IC12	7442	16	8
IC13	74123	16	8
IC14	7438	14	7
IC15	7400	14	7
IC16	74L04	14	7
IC17	S2350	2	1

Note: 74LXX and 74LSXX types may be replaced by 74XX; 8097 may be replaced by 8T97.

Instruction Latch to Disk Drive

Execution of an OUT 243 causes the contents of the 8080's accumulator to be loaded into IC5 and IC6. The 5 least significant bits are used to send the low speed control signals to the disk drive. Table 1 shows the allocation and the polarity of these bits as they appear in the accumulator. The three most significant bits are used by IC7 to select one of up to eight different drives which may be attached to each interface.

Status Load from Disk Drive

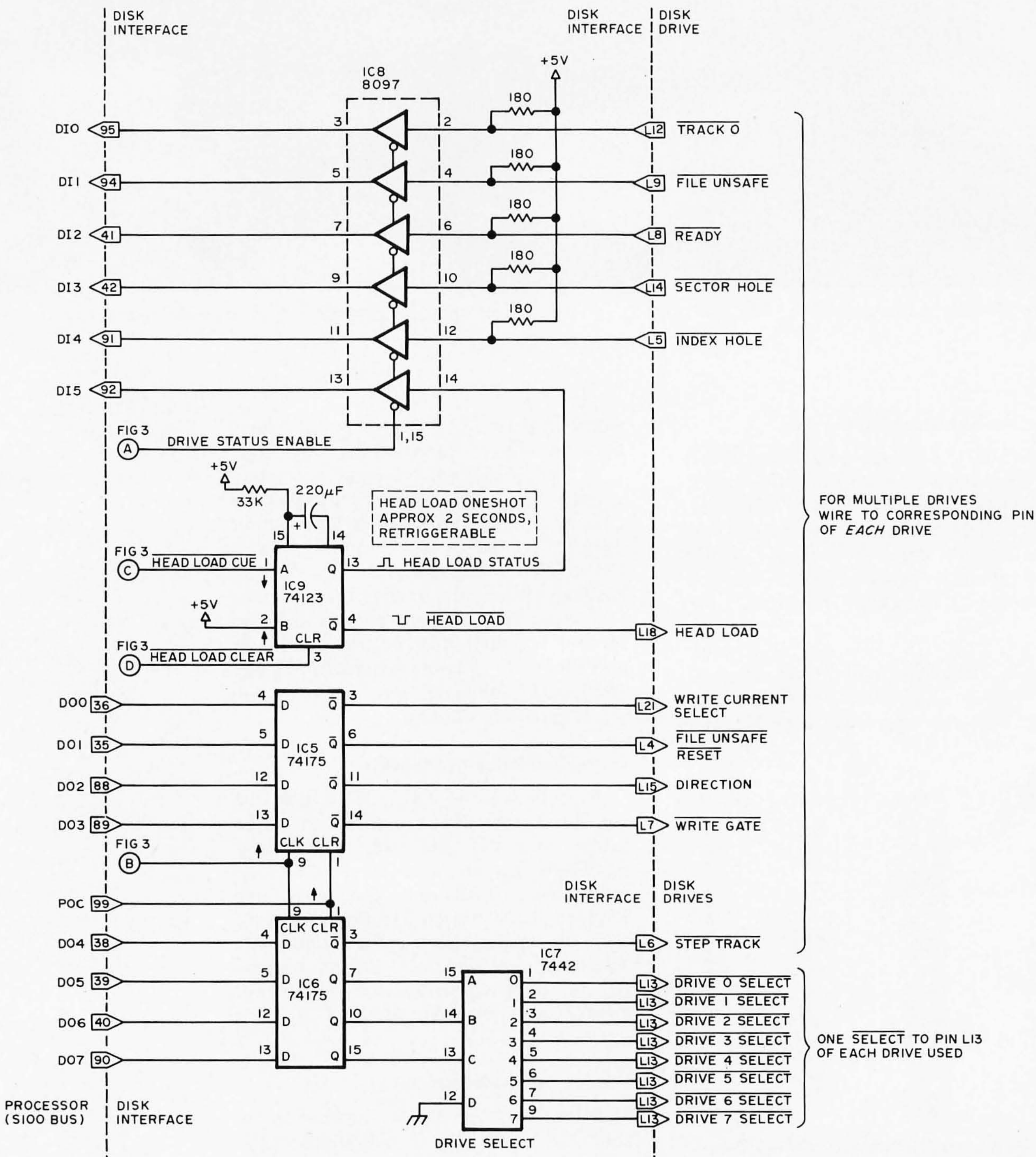
Execution of an IN 241 instruction enables IC8 to load the current status of the selected disk drive onto processor input data

lines DI0 to D15. Table 2 shows the allocation and polarity of these bits as they are loaded in the accumulator. The two most significant bits are unused, and will always show 1s.

Head Load-Unload

IC9 is a retriggerable one shot with a 2 second pulse width. Executing an OUT 245 instruction initiates this pulse and loads the disk drive head, regardless of the contents of the accumulator. If another OUT 245 instruction is executed within 2 seconds of the first OUT 245, then the head will remain loaded for a further 2 seconds. The head will unload 2 seconds after the last OUT 245

Figure 4: This diagram shows the circuitry used to perform all of the low speed functions of the disk drive. IC8 is a 6 bit input port, and IC5 and IC6 are an 8 bit latched output port. IC7 selects one of up to 8 disk drives on the system, and IC9 controls the loading of the disk's data transfer head for a read or write operation.



(load head) instruction. This 2 second pause allows the head to stay loaded during successive reads and writes to the disk, but will automatically unload the head after 2 seconds without any disk activity. Alternatively, an OUT 246 instruction will cause the head to be unloaded immediately if and when that is desired. This automatic head unload feature minimizes wear on the floppy disk. If it were not present in some hardware or software form, the head would be continuously in contact, wearing out disks quite quickly if your machine ran 24 hours a day.

The USRT

The abbreviation USRT stands for Universal Synchronous Receiver Transmitter; this chip really is quite universal. Although it was originally developed for data transmission over phone link, wire link, and some types of tape drive, the S2350 USRT performs all of the needed high speed data transfers to and from the disk with almost no modification. Before discussing the operation of the USRT transmit and receive sections of the interface as a whole, take a look at the functions of the USRT itself, as

TDS Transmit Data Strobe

An OUT 240 instruction of this interface puts a pulse on the TDS line which loads the accumulator into the USRT transmitter buffer through processor data output lines TD0 to TD7. The USRT then shifts this data byte out onto TSO (Transmit Serial Out). One bit is shifted onto TSO for each pulse on TCP (Transmit Clock Pulse).

TBMT Transmit Buffer Empty

Whenever the transmitter buffer is ready to receive another byte (from an OUT 240 instruction), the TBMT line goes high.

TFS Transmit Fill Strobe

An OUT 241 puts a pulse on the TFS line which loads the accumulator into the USRT fill buffer. If new data is not sent to the transmit data buffer by an OUT 240 soon after a TBMT signal, then the USRT has no data to send out on the TSO line. In this case, data from the transmit fill buffer is sent out in place of the missing data.

RSS Receiver Sync Byte Strobe

An OUT 242 pulses the RSS line which loads the accumulator into the USRT sync byte buffer, for use at the beginning of a data read operation.

RR Receiver Reset

An IN 243 causes the receiver section of the USRT to be reset into the "Search for Sync Byte" mode. The received serial data stream enters on RSI (Receive Serial Input), and is clocked into the received data buffer by the RCP (Receive Clock Pulse) line. When the data byte in the received data buffer matches the byte in the sync byte buffer, the RDA (Received Data Available) line goes high. After this happens, a new byte is put into the received data buffer after every eight clock pulses on RCP.

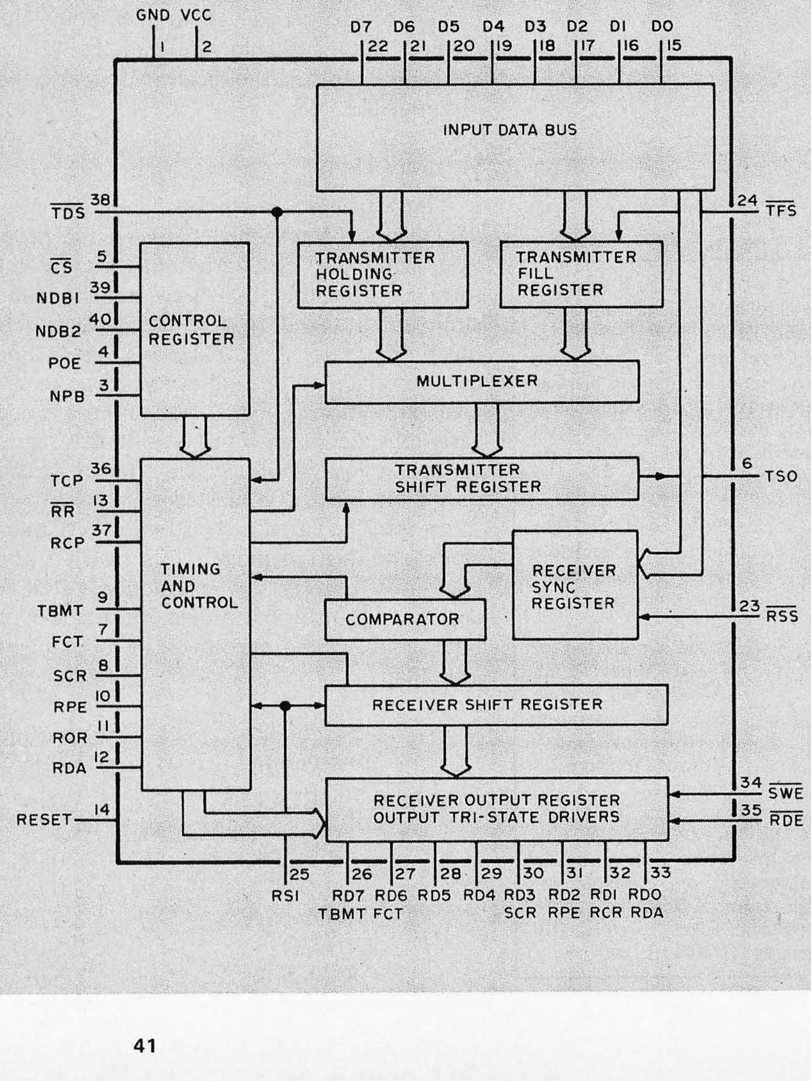
RDE Received Data Enable

An IN 240 instruction pulses the RDE line. This puts the data in the USRT received data buffer onto data lines RD0 to RD7, and it is loaded into the accumulator. In this manner, the 8080 brings in the data read from the disk.

SWE Status Word Enable

An IN 242 pulses the SWE line which loads the USRT status word into the accumulator to examine for data ready, or to find possible errors.

Figure 5: This is a block diagram of the USRT integrated circuit, the AMI S2350. The information here is redrawn from the original contained in AMI's data sheet on the device. The USRT integrated circuit is the heart of this inexpensive floppy disk interface, performing all of the high speed data manipulations needed to read and write data from and to the disk drive. The USRT was not intended to be used as a floppy disk interface when it was originally designed. But as demonstrated by this article, a little ingenuity can often come up with surprisingly versatile applications of standard integrated circuits for use in high speed data communications.



denoted by the various signal lines. Figure 5 shows a block diagram of the S2350, along with captions detailing these lines and their relation to the interface as a whole.

USRT Transmit

After the disk drive head has been loaded and the desired track and sector found, the write gate is turned on and data from the processor may be sent to the transmit section of the USRT through an OUT 240 instruction. IC11 divides the Altair 2 MHz clock by 8 to give the 250 kHz clock required by the disk drive. This clock is fed into TCP, and IC12 combines the data from the transmitter serial output line and another clock phase into the proper write data format required by the disk drive as seen in figure 2.

USRT Receive

IC10 is simply used as a pulse stretcher for the separated data and separated clock from the disk drive. The data pulse is expanded to overlap the falling edge of the clock pulse. This overlap allows the data to be read properly by the USRT. When a byte of data has been received (as denoted by the receiver data available line), an IN 240 instruction will load the received data into the accumulator.

Software Timing

The article to this point has shown how data can be transferred between the processor and the disk drive in the correct format, but nothing has been said about the ability of the 8080 to send or receive data at the proper rate. A 250 kHz bit rate is one byte of data in or out every 32 μs under ideal conditions. If the drive motor speed variations are taken into account, this figure can be as low as 30 μs per byte on a read operation. Since 8080 instructions take from 2 to 7 μs to execute (assuming a 2 MHz clock and fast memory), this restricts the read loop to very few instructions. If it is desired to transfer more than 256 bytes in or out at any one time, the read loop might look like:

	Symbolic Instruction	Execution Time
LOOPA:	IN STATUS	5.0 μs
	ANI DATAREADY	3.5 μs
	JZ LOOPA	5.0 μs
	IN DATA	5.0 μs
	MOV M,A	3.5 μs
	INX H	2.5 μs
	DCX B	2.5 μs
	MOV A,B	2.5 μs
	ORA C	2.0 μs
	JNZ LOOPA	5.0 μs
		36.5 μs

In the above example the HL register is used to point to the data buffer, and the BC register is the number of bytes to be read. The total time of the loop, 36.5 μs, is 6.5 μs too long for the worst case data read. Obviously this program will not read data in properly.

By eliminating two lines of code the loop is reduced to a total time of 28 μs as shown in the following example. This is quite ample for the interface and allows additional leeway for the possibility of dynamic memory's introducing a wait state during the loop.

	Symbolic Instruction	Execution Time
LOOPB:	IN DATAWAIT (IN 244)	5.0 μs
	IN DATA (IN 240)	5.0 μs
	MOV M,A	3.5 μs
	INX H	2.5 μs
	DCX B	2.5 μs
	MOV A,B	2.5 μs
	ORA C	2.0 μs
	JNZ LOOPB	5.0 μs
		28.0 μs

Obviously this version of the routine will not work without some special "trick." In this case, the trick is that the first three lines of LOOPA have been replaced with the first line of LOOPB and some special hardware. The first three lines of LOOPA prevented the IN DATA statement from reading data before data was available. In LOOPB, the IN DATAWAIT is an IN 244 instruction. This triggers IC13b, a one shot, which puts the 8080 into a slow memory wait state by pulling the Altair's PRDY line low. When data is ready for input, the RDA line of the USRT resets IC13b and allows the LOOPB routine to continue. During normal execution of a read operation, the 8080 does a 4 μs wait between lines 1 and 2 of LOOPB. This wait state serves to synchronize the reading of the disk data with its availability. Any amount of data from a partial segment to an entire track may be input with this routine.

If some hardware failure should occur, and data stops coming into the USRT, then RDA will never go high. If no data arrives after 3 ms, then IC13b completes the one shot cycle and releases the 8080 wait state. This feature prevents a hardware failure in the disk drive or interface from hanging the

A printed circuit board is available for the advanced hobbyist to construct his or her own interface. The printed circuit board fits into a single Altair (or generic equivalent) slot, and supports the circuit described in this article with two additions:

1. Eight head load circuits allow multiple drives to load heads simultaneously.
2. Space is provided for a 1702 type PROM, to allow the user to load the operating system from the disk without toggling in any data.

The printed circuit and documentation only (no ICs or sockets) are available for $35 from K B Welles, 2623 Fenwick Rd, University Heights OH 44118.

processor up in an endless wait state. Whether a read operation is successful or not, the end of the loop is reached when the BC register pair's count is decremented to zero and the JNZ condition no longer pertains.

In order to write data, a software output loop similar to LOOPB is employed:

	Symbolic Instruction	Execution Time
LOOPC:	OUT DATAWAIT	
	(OUT 244)	5.0 µs
	MOV A,M	3.5 µs
	OUT DATA	
	(OUT 240)	5.0 µs
	INX H	2.5 µs
	DCX B	2.5 µs
	MOV A,B	2.5 µs
	ORA C	2.0 µs
	JNZ LOOPC	5.0 µs
		28.0 µs

With this output loop, the 8080 can maintain the data rate required to transmit data to the disk properly. A similar hardware synchronization trick is also used in this case.

Final Hardware Notes

The circuit shown in figures 3 and 4 was developed for use with an Innovex 220 drive. The 220 has multiple options which can be selected by jumpers on the circuit board. The options required for use with this interface are:

1. Radial Interrupt Disabled (Link E installed)
2. Radial Rotation Sensing Disabled (Two Link Es installed)
3. Read Data Option Disabled (Link A installed)
4. Write Protect Option Disabled (Link H installed)
5. Stepper Power Option (Link E installed)
6. Radial Head Load Disabled (Link E installed)

The selected options allow multiple drives to be used with the interface. While up to eight disk drives can be connected in parallel (with the exception of the device select lines), the shorting clip on the P07 line must be removed from all but the last disk drive on the bus (P07 connects the bus termination resistors to +5 V). In addition, the user must provide power supplies for the following voltages and currents:

+5 V, 800 mA for each drive
−5 V, 75 mA for each drive
+24 V +/−2 V, 1.4 A for the first drive, 0.1 A more for each additional drive

Conclusion

The small number of ICs in this circuit (17) and their low cost and easy availability puts the construction of this circuit within the abilities of many intermediate and advanced computer hobbyists and experimenters. The addition of a disk drive to the average home system will increase the overall system usefulness many times. By reducing the time required for software generation to a fraction of that on a cassette or paper tape system, software throughput and sophistication of the typical personal computing user (and professional) will typically double or triple.

I currently have two drives running on an Altair system, and a complete disk operating system existing in 2 K of PROM that allows operating with up to 240 different named files on each disk. Loading BASIC takes only 6 seconds, and loading STARTREK using CLOAD takes only 3 more seconds. The disk drive and operating system has increased software generation at least fourfold, and made the system much more enjoyable to use.■



Color Displays on Black and White Television Sets

Steve Bain
Technagraphic
POB 5014
Arlington TX 76011

Figure 1: The Benham Disk. When rotated clockwise at 5 to 10 revolutions per second, the black arcs nearest the center appear to be red, the middle arcs appear to be green, and the outer arcs appear to be blue. If the direction of rotation is reversed, so is the order in which the colors appear.

Add Subjective Color to Your Video Interface

Interest has been growing in the idea of using standard color television receivers as microcomputer output devices. At least one color television interface is already commercially available and more are on the way. In addition, many homebrew projects are ongoing.

There are, however, problems with using home color televisions as output devices for microcomputers. Most hobbyists' color televisons are dedicated to pastimes such as Walter Cronkite and "The Waltons." The family may not enjoy relinquishing its viewing rights while that new program is being debugged.

More serious are the technical problems involved. National Television System Committee standards were designed to compact the maximum amount of useful color information into the minimum bandwidth. The standards accomplish this goal well, but they require that the color information in the video signal be highly encoded. Hence the hobbyist must either encode his color data or extensively modify his set. Also there are the traditional color television bugaboos of convergence and excessive X-ray exposure to consider, since the average viewer to screen distance for most computer IO applications is likely to be less than the viewer to screen distance for conventional viewing.

One can also brood over the inherent resolution limitations of National Television System Committee color television. The National Television System Committee, as you may recall, was the engineering group which developed US color television specifications. If high speed memory prices continue their expected decline, the cost of storing a high resolution picture will become insignificant when compared with other system costs. The personal computing experimenter may find that the resolution of his computer graphics is limited only by the construction of his CRT and the bandwidth of its driving circuitry. For standard color televisions the chrominance bandwidth is much less than the luminance bandwidth and thus the color change resolution is rather limited. Even if the color picture tube were to be driven by high bandwidth circuitry, color change and intensity change resolution would still be limited to about $500 \times 500 = 250{,}000$ points by the shadow mask inherent in the tube. Of course, it is possible to build a higher resolution shadow mask tube, but one must remember that color picture tubes are affordable only because they are mass produced. There is currently little demand for high resolution color tubes.

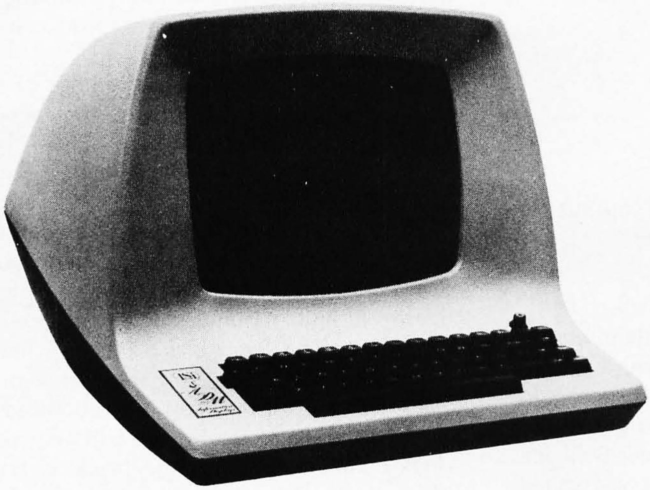
The preceding discussion is not an attempt to quench the reader's desire to have his microcomputer spew data in living color. A look at the impressive outputs from the Cromemco or Intecolor devices would rekindle this desire anyway. The discussion is intended only as an effort to legitimize the search for an alternative. Is there a viable alternative to standardized shadow mask

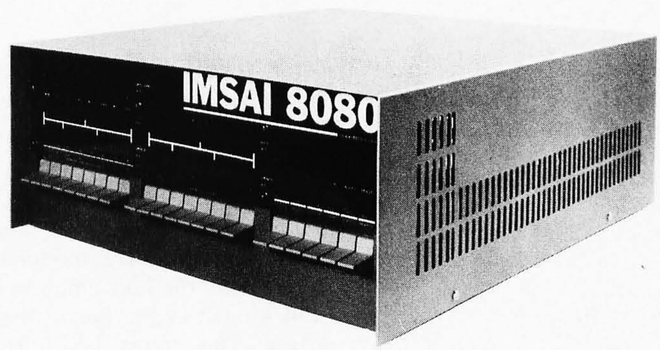
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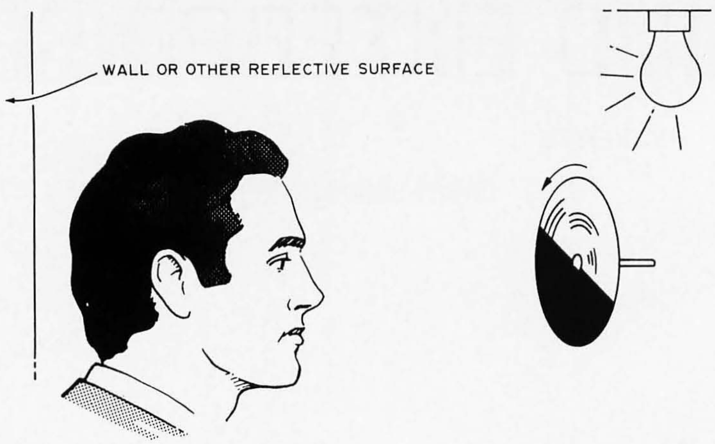


Figure 2: A suggested geometry of illumination for viewing the Benham disk.

color for real time computer output in color? The surprising answer is yes!

Subjective Color . . .

There is a long known but little discussed method of making black and white images which are properly modulated appear in color. This method employs an optical illusion known as the Prevost-Fechner-Benham effect. The colors which result are called Fechner's colors or subjective colors.

One can modify most video display interfaces or television typewriters to produce subjective color output on a standard black and white television. The modifications are entirely electronic and do not involve moving filters, special glasses, or Rube Goldberg mechanical contraptions. Most viewers agree that the colors which are produced, although not competitive with NTSC colors in saturation and brilliance, are impressive.

Subjective color television does have its limitations, however. It works best in producing sensations of the primary colors: red, green and blue. Other colors can be produced, but only at some loss in saturation. Subjective color can be made to appear only in relatively small areas of the screen which lie against a white background, but this is not a significant problem in most computer IO applications. For instance, one cannot cause the entire screen of a black and white TV to appear in a subjective red. However, one can cause red, green or blue dots, lines or letters to appear against a white surround. Finally, due to the nature of the modulation which produces the illusion of color, subjective color images have a noticeable flicker.

. . . And Its Origin

The Prevost - Fechner - Benham effect is named after its discoverers and developers. Benedict Prevost was a French monk who in 1826 discovered that a black and white object which was moved through a beam of light in a darkened room could produce a variety of colors. G T Fechner, a German physicist, developed a disk in 1838, with black and white areas which produced subjective colors when rotated. Subjective color was not heard from again until 1894 and 1895 when C E Benham published papers on "The Artificial Spectrum Top" in the journal, *Nature*. Benham developed a disk that is particularly efficient in producing subjective colors and it is reproduced in figure 1.

Just as there is a small percentage of the population which is colorblind, some people do not see subjective color. These two groups of people do not coincide. Some otherwise colorblind people see the entire spectrum of subjective colors. To find out if you can see subjective colors, draw your own Benham disk or make a photo copy of figure 1 and mount it on a piece of cardboard. The large black area will likely not photo copy well, so darken it with a black felt tip marker. You may also need to go over the black arcs with a ballpoint pen. High contrast between the black and the white areas of the disk will produce the best subjective color. Stick a straight pin through the center of the disk and cement the head of the pin to the topside. Then go into a room that is lit by incandescent lamps and rotate the disk between your thumb and forefinger at approximately five to ten revolutions per second. Experiment with slightly different speeds until you see the colors listed in the caption to figure 1. I have found that the geometry shown in figure 2 is one of the best for viewing the disk if a single source is used for illumination. Notice that the light as well as the disk is within the field of vision.

It must be emphasized that subjective colors do not result from any change in the wavelength distribution of the light which is reflected from the disk. If a one second time exposure were to be made of a spinning Benham disk on color film, the result would be a light grey disk with dark grey circles. The colors result from a temporal optical illusion. Television makes use of another temporal optical illusion: The flicker fusion which causes single frames shown in rapid succession gives the appearance of continuous movement on the screen. The explanation of subjective color is probably partly psychological, due to the mental interpretation of black and white areas of contrast, and partly physiological, due to the differing response and decay times of various color receptors. However, the precise reason for the effect remains unknown.

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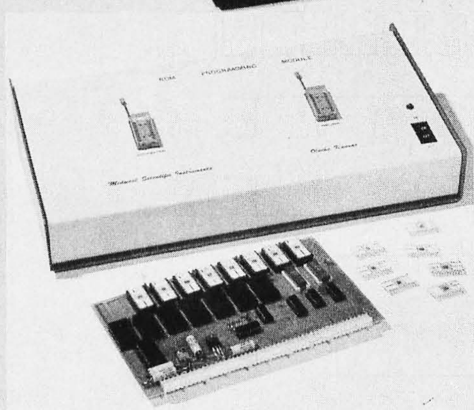
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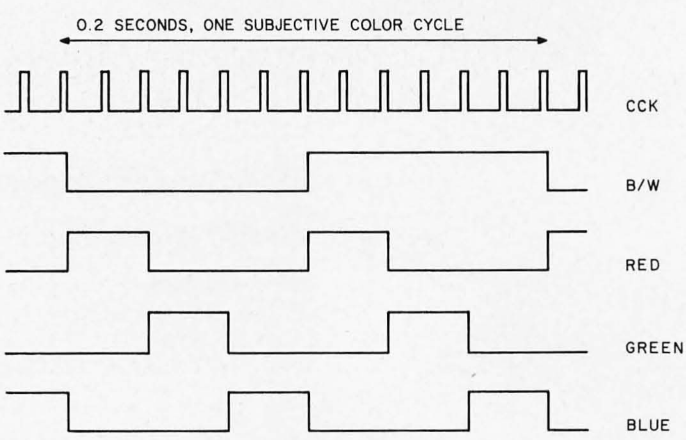
The Color Code . . .

Just how does one go about adding subjective color to a video display? Unfortunately, the large number of varying video display interfaces and television typewriters which are now available make it impossible to give a single cookbook approach. Thus, it will be explained rather precisely what the effects of the modifications must be and then some general suggestions will be given as to how to implement these effects. The rest is up to the reader. Suggestions will only be directed toward the goal of implementing the primary colors. Nonprimary colors can be produced, but the results are less impressive and the price is a considerable increase in the complexity of the necessary modifications.

American computer hobbyists are fortunate in that the 30 frames per second NTSC standard supports subjective color almost optimally. The European standard of 25 frames per second is much less attractive.

The code which produces subjective color can be read from a Benham disk. Think of the television display in terms of subjective color cycles. Each such cycle lasts for one fifth of a second and comprises six complete video frames, each lasting one thirtieth of a second. One cycle corresponds to one revolution of a Benham disk. For the first three frames of each subjective color cycle, the entire CRT display must be black. During the fourth frame only those portions of the display that you want to appear as red should be black. The rest of the display must be white. During the fifth frame, those areas of the screen that you want to appear as green should be black and the surrounding display should be white, including the areas that were black during the fourth frame. During the sixth frame those areas that you want to appear as blue should be black. The rest of the display should be white. A new cycle should then begin with the start of the very next frame.

There is one exception to the code given above. Those portions of the display that you want to appear as black should be black during all three of frames four, five, and six of each cycle.



CS1	CS2	COLOR
0	0	BLACK
1	0	RED
1	1	GREEN
0	1	BLUE

Figure 3: Subjective color timing pulses.

. . .And Its Implementation

Now for some suggestions as to how to implement the subjective color. Comments will be directed toward some idealized reader who is familiar with television terminology and who has a video interface which produces typical television display functions. That is, it produces dot matrix characters on a conventional black and white television from ASCII coded input. However, many of the suggestions will be useful in graphics oriented applications as well.

It is possible that some currently available or soon to be available video interface is so versatile that subjective color can be implemented using software alone. Our discussion will be directed toward its implementation with hardware.

Most video interfaces are set up to provide white dot matrix characters against a black surround. Subjective color requires black characters against a white surround. This requirement suggests that interfaces which support interlacing are to be preferred for this application over those that do not. Unfortunately, the popular low cost interfaces such as Southwest Tech's TVT II and Processor Technology's VDM-1 do not interlace since doing so would greatly complicate their timing circuits. Luckily, a lack of interlacing is not a serious problem in the creation of subjective color for typical viewer to screen distances. Use of a small monitor minimizes the effect of dark spaces between lines.

VDM-1 can provide a black on white image under software control. With other interfaces, providing this feature may be as simple as inverting the output of the character generator's shift register. However, it is conceivable that doing so could affect the generation of the vertical and horizontal sync pulses so check the circuit diagram of

Continued on page 116

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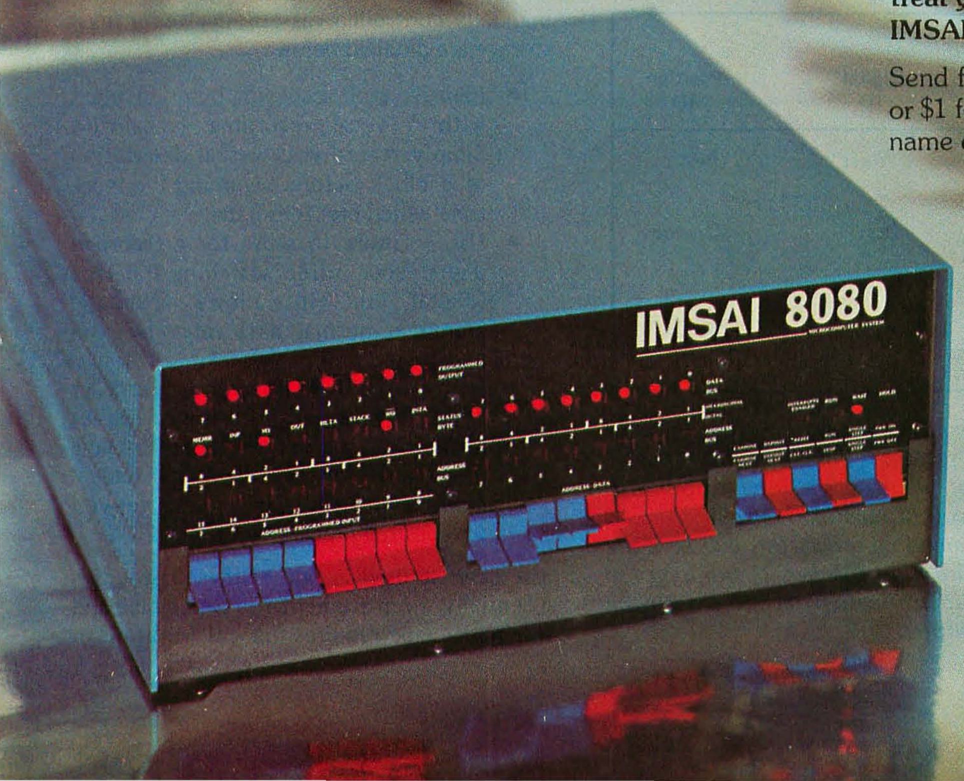
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Serial Storage Media:

An Introduction and Glossary

Brian D Murphy
72 Circuit Dr
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Brian Murphy *has been professionally involved in the computer business for more than eight years, at all levels of programming and usage. His experiences range from scientific and simulation software on large machines to the world of personal microcomputers. He is currently employed by the US Navy.*

This is an introduction to the use of a cassette type recorder for mass storage of information. Once the initial novelty of the small computer system has worn away, a junction occurs at which the computer freak either matures or puts his (or her) system on the market and moves on to something else like stamp collecting. If a person has a valid interest in the uses of computer technology, however, he or she soon finds self in a bind as regards the permanent or semi-permanent storage of programs or data on something more easy to transfer into his/her computer than paper. If a hobbyist is limited by funds (or by spouse), he or she soon learns that the only media suitable for his/her storage is magnetic tape utilizing a cassette recorder. He/she now has available a primitive serial access device. The word "serial" has the same root as "series," which means (in a very loose definition) one thing following on the tail of another. If you walk down a corridor to a particular room you are applying serial access to the problem of locating the room you want to enter: Each door is passed in turn. Thus serial access is quite different from random access (such as in your computer's memory), where you arrive immediately at your destination (similar to teleporting yourself directly to the room you wish to enter). One goal of this article is to familiarize the novice reader with the computer industry concepts and terminology. To this end, we include a glossary that will hopefully define those terms with which you may not be familiar. Also included is a book list for your bedtime reading pleasure.

Technique / Characteristic	Vocal ID	Digital ID	Position ID
Access Time	Medium	Worst	Best
Amount of Manual Interaction (Play, Rewind Pushing)	Worst	Best	Medium
Tape Utilization (Minimum Wasted Tape)	Medium	Worst	Best

Table 1: Comparisons of Manually Controlled Cassette Information Management Techniques. A rudimentary file storage system is possible with manually controlled cassettes, essentially variations of what people used to do with paper tape file systems. A file system is a way of locating logically grouped records in the mass storage medium. For manual recorders this can be done by listening for voice identifications through a loud speaker, by running the tape and matching against a desired block identification recorded with the records, or by looking at the tape position counter.

A cassette type recording medium is the most economically attractive alternative for the small system at this time. The cassette recorder as it comes off the dealer's shelf, however, is awkward to use in a computer system. There are three general methods, appealing because they are inexpensive, available for using such a device. The three general filing system methods for using a manually controlled cassette device for mass storage are detailed below:

- Identify each recording by prefacing it with a vocal recording (vocal id). Simply record your verbal description of a block before beginning the mark tone which precedes data.
- Use software to sense for a recorded digital code while searching the tape (digital id). This allows automatic search at normal data rates, but can take a long time.
- Buy a more expensive audio recorder with a mechanical position readout and maintain a written record of tape usage (position id). Here the manual cuing controls of the recorder get you to a desired block very quickly.

The cassette used in one of these fashions is essentially a replacement for paper tape and like paper tape requires manual (or at most,

automatic motor control) operation. Each of these techniques has its own advantages and disadvantages as shown in table 1.

As the personal computing user becomes more sophisticated, he or she will soon find a need to have an electronically controlled recorder available for his/her use along with software of a more sophisticated file system. Such a software controlled recorder can automatically search the tape for a requested recording, going forward or backward as required, and loading in the desired data. The file system is a neat software utility that can operate separately or, for the more advanced, as part of an operating system. The remainder of this article will acquaint the novice with some of the characteristics of automatically controlled serial storage and the tradeoffs and physical considerations inherent in its nature. No attempt is made to go into the much larger subject of file systems.

As was mentioned previously, searching for a particular item in serial storage requires looking (humanly or via software) at identifying material that accompanies the desired recording. For tape media, the looking proceeds in a serial fashion until the desired record is located. A record is a group of bytes or words representing the data stored. The time that it takes to locate the desired record is called access time, and in measuring the efficiency of the device in general, average access time. A serial device has an access time of T*(N−1) to find the Nth record, if all records are the same length and the time to get to the second record is T. If the records are of variable length, the access time will be the sum of all the times to pass by each preceeding record. The average access time would be the time it takes to search half the recorded tape. The software must have a way to tell one record from another, or in fact when one record ends and another begins. In a simple record file system, each record is preceeded by a tape mark which signals the start of a record. Tape marks are distinctive in nature and are composed, for example, of a number of special characters of predetermined count (the ASCII SYN character is sometimes used). Following the tape mark is identifying material, and the record itself followed by a checksum (see the glossary). A sample layout of a typical tape (or format) is shown in figure 1. Associated with each recording are inter-record gaps. The gaps are areas on tape that contain no meaningful data. They exist due to the physical limitations of the recorder and represent the time the motor takes to start or stop. These "gap waste" and may consume a considerable amount of the tape of an unwary user.

To appreciate the impact of gap waste it is necessary to understand the physical aspects of the recorder and tape medium. The amount of information that can be recorded or read during a given time is determined by the transfer rate of the recorder. Transfer rate is measured in bits per second (bps) and is a function of recording density, tape speed, and the recorder electronics. The recording density is the number of bits that are stored on one inch of the tape, measured in bits per inch (bpi). Now we can relate inter-record gap to a physical situation. Suppose we have a recorder with a transfer rate of 2400 bits per second and a motor start or stop time of 0.5 seconds, with a linear speed change during that interval. This is a model which demonstrates the problem of gaps; in actual systems the start time might differ from the stop time, and the curve would probably not be linear. Using this simplified model, since the stopped rate is 0 inches per second, and the "started" rate is the full tape speed, the linear speed change implies an average speed of the tape during the interval change which is exactly half of the full speed. Thus, during the transition interval, exactly half of the tape which would have gone by at full speed

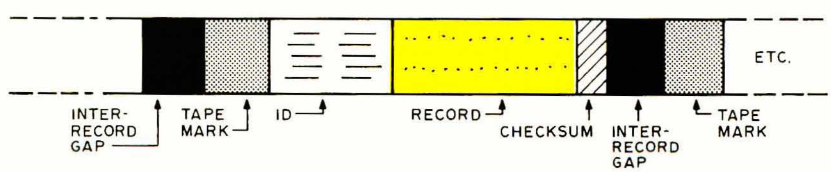


Figure 1: Format of a Typical Magnetic Tape Record. This diagram can be viewed as a timing diagram (from left to right), or as its equivalent, a physical map of a tape which is moved past a fixed head from left to right. In this conception, a record is preceded by an inter-record gap, followed by a software (or hardware) coordinated tape mark for synchronization, then (if a file system is employed) some software identification information and finally the data of the record. A trailer of a checksum is often used for error detection, after which an inter-record gap precedes the next item on the tape.

is wasted in the gap. At full speed, with a 2400 bps transfer rate, 0.5 seconds would have recorded 1200 bits, so the tape which is lost to the gap during speed changes corresponds to 600 bits in this case, or 75 bytes. Since each record is surrounded by a startup leader and a slowdown trailer, the total gap is the sum of these components, or the length of tape which would have stored 75+75=150 bytes in this particular model. This should be a clue as to why small physical records are wasters of tape. Consider a logical print line record of 72 characters (fixed length) which is to be stored on tape for later use with a Teletype or its equivalent. If I were to store 72 bytes per physical record, making the logical and physical record equivalent, then each record would occupy the space on tape which could

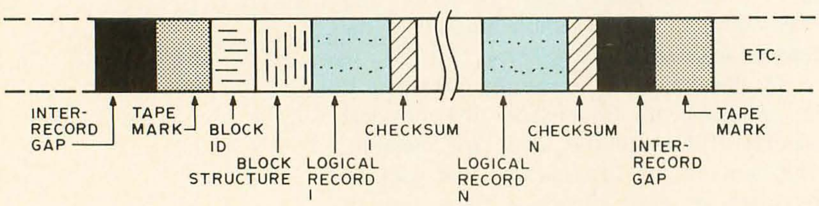


Figure 2: A Blocked Magnetic Tape Format. Instead of immediately ending the recording operation, the physical record can be formatted to contain multiple logical records, so that the number of gaps required is reduced. Blocking is a very common software practice whenever computers get large enough to allow several thousand bytes to be used for IO buffers in which the blocked records can be built and decoded by software.

Characteristic \ Type	Blocked	Unblocked
Tape Utilization	Higher*	Lower
Access Time	Faster*	Slower
Software Complexity	Higher	Lower*
Computer Memory Needed to Process	More	Less*
Computer Time Needed to Process	Longer	Shorter*

Table 2: A Comparison of Blocked versus Unblocked Record Formats. This table identifies general qualitative characteristics of the two forms. The asterisks identify qualities which are often desirable.

GLOSSARY

Access time: The time required to locate a particular record on the storage medium.

Average access time: The amount of time required, on the average, to locate an item on the storage medium. On tape the average time is the time it takes to search half the recorded tape.

Blocking: A method for collecting logical records into a single physical record on the storage medium, thus minimizing inter-record gaps.

Checksum: A value calculated from the data which is used to help determine if data transferred from one medium to another is correct. If a record is read from tape and a temporary electronic error occurs that alters the data being sent, the checksum may signal an error. A simple checksum is generated by treating each byte or word recorded as a number, adding each such byte or word into a total as it is recorded. Overflow is ignored, and the final total is recorded on the tape with the record. This particular method, while simple, is not foolproof. Many more elaborate techniques exist which even allow for correction of an error. The same procedure is followed on subsequent reading of the record, and the final total is compared against the recorded checksum. If the two values do not match, an error has occurred.

Format: The manner in which data is grouped to allow organized access and handling of the data.

Gap waste: The amount of storage space wasted by inter-record gaps.

Inter-record gaps: That portion of unused tape surrounding the beginning and end of a recorded section of tape. The gap exists due to the nonzero startup and stop time of the recorder's motor.

Logical record: A contiguous recording of a block of bytes or words that has a separate identity. An example of a logical record is the recording of one program.

Physical record: Also a block, this term refers to a continuous collection of logical records grouped together without gaps. The purpose of the physical record is to conserve storage medium. One physical record might conceivably have multiple logical records, or only a portion of a logical record.

Record: A record is a string (or block) of data recorded on the medium that is separated from other records by inter-record gaps.

Recording density: The number of bits stored on one inch of tape. The units of measurement are bits per inch (bpi).

SYN: The "synchronization" character. It has the ASCII hexadecimal value 16.

Tape mark: A distinctive recording at the beginning of a tape record signaling the beginning of a record. It must be distinguishable from data to avoid confusion.

Transfer rate: The number of bits per second (bpi) a given device can transmit. In commercial drives, this rate varies from design to design, even given identical recording density and format. For audio recording of data, it is largely a function of the interface modulator and demodulator and for the most part is independent of the tape recorder.

store 72+150=222 bytes if the gap were not present. The utilization of the tape is thus 72/222 or about 32%. If, instead of a 72 byte physical record, we use some IO software and a blocking factor of (for example) 25 logical records per physical record, physical space on the tape for each record is 1800+150 or the equivalent of 1950 bytes, which has a utilization of 1800/1950=92%. Thus the answer to maximizing the use of tape space is to be found in the practice of blocking and the use of file systems with moderately large buffer areas in memory.

Blocking is this practice of grouping multiple logical records into each physical record. Suppose you have a number of small records to save and want to eliminate gap waste as much as possible. By creating a "block," which is a contiguous group of records, you can treat the block as a large physical record which is in reality composed of a number of smaller logical records, as in figure 2. Each logical record is one of the individual records that you originally wished to store. Now there will be gap waste only around the physical records (blocks), and thus the wasted tape will be greatly reduced. The problem now becomes one of finding the correct block and locating the proper logical record within it via software. The mechanism which allows you to do this and other neat things like calling records by alphanumeric string names is the file system. However, blocking is not without disadvantages, not the least of which is memory requirements. In big systems, block sizes often range into the thousands of bytes, and various "multiple buffering" techniques require alternating regions. In a large IBM/370 program (say 100 K to 200 K bytes) it is not uncommon to find 30 K to 50 K bytes used only for buffers: Some of the pros and cons of record blocking are shown in table 2.

Armed with the information in this short tutorial and glossary, the novice reader, it is hoped, will have a better appreciation of the concepts of information storage adapted for inexpensive computers. ■

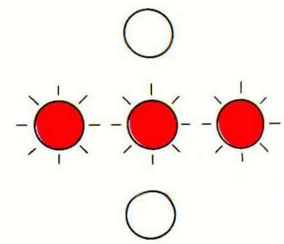
SUGGESTED READING

These books are contemporary texts, which should be available at most good technical libraries and college book stores.

Operating Systems: a pragmatic approach, Harry Katzan Jr, Van Nostrand Reinhold Co.

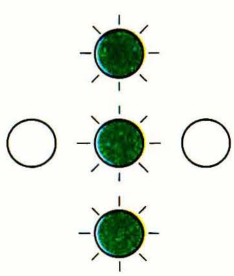
Systems Programming, John J Dovovan, McGraw-Hill.

Computer Organization and Programming, William C Gear, McGraw-Hill.



Audible Interrupts for Humans

Dr Charles F Douds
381 Poplar St
Winnetka IL 60093



One of the great virtues of computers is that their flexibility allows them to do all kinds of things to make our lives easier or better.

Unfortunately, systems analysts and programmers working on big systems sometimes tend to forget this. Microprocessors can make things easier and more fun for us, too. But we sometimes forget the basic principle of human engineering: People should not be forced to fit the system; the system should fit the people.

I almost forgot this when I was developing my hardwired process control system. The design philosophy behind the whole system was that it was to take over certain jobs that the human operators were not interested in doing, while other more interesting jobs remained the operators' responsibility. There was no intention to make it a fully automatic system. This fits principles of good human engineering, but in the details I overlooked something.

An output from the original system presented a visual display to the operator. One state indicated that he could proceed as he wished; the other state indicated that he must come to a stop. A clearly visible display was provided. The display consisted of a set of three vertical LEDs for go, and three horizontal ones for stop. The only trouble was that when people began using the system, they were often going when they should be stopping.

What I had overlooked was that the operator would be, quite properly, watching the equipment he was running. Only when the LED display happened to be within his line of sight would he respond to them.

To remedy this situation I could have hollered at the operators until they learned to watch the display as well as their equipment; or I could have used another one of their sensory inputs. The first choice does use a sensory input other than vision. Why not just automate my hollering? That is what I did; only the end result sounds a lot better. Not only that, it provides additional information as well. It also indicates when the signal has cleared.

What I did was to build an audio annunciator that is triggered by the same line that drives the display. When the line goes high, the device emits a one second beep. When it goes low, a boop sounds. Beep for stop; boop for go. It worked out quite well.

The Circuit

The audio burst is generated by two 555s or one 556 timing IC. IC2 is wired as a oneshot to determine the tone duration. The time is set by C4 and R11. A negative going pulse on input pin 2 triggers the oneshot on. If your circuit creates a pulse, rather than a level change, the input should be connected here.

The tone is generated by IC3. Its frequency is set by C5, R13 and R14. The ratio of R13 to R14 determines the pulse width. Diode D3 helps to provide more nearly a square wave. If pin 4 is connected directly to VCC temporarily, you can pick the resistor combination that gives the most pleasing tone. Connecting R15 from the output of the oneshot into pin 4 allows the free running oscillator to be turned on for the duration

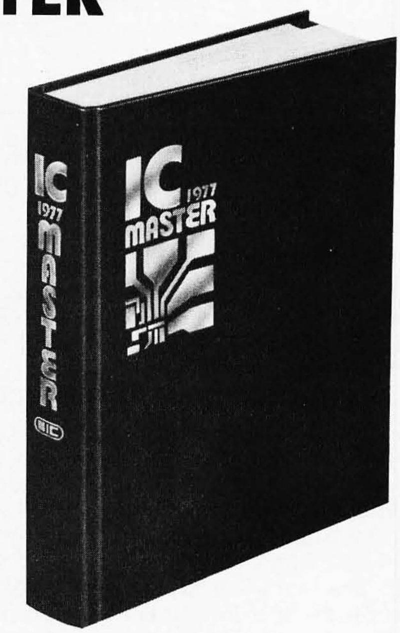
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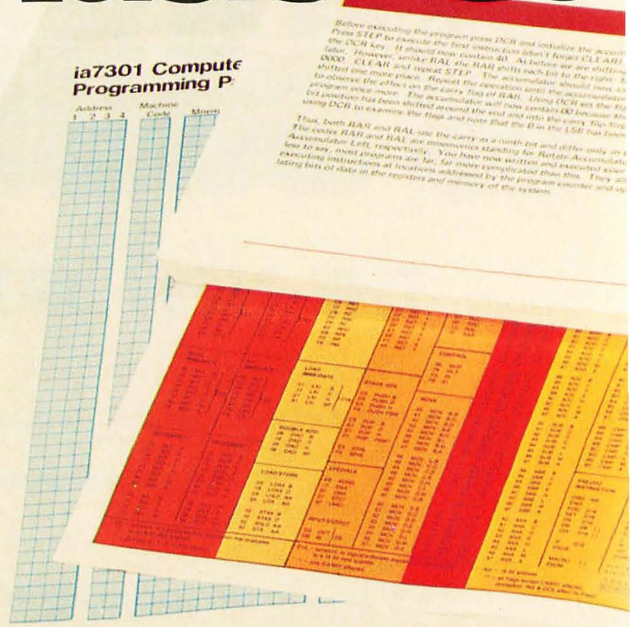
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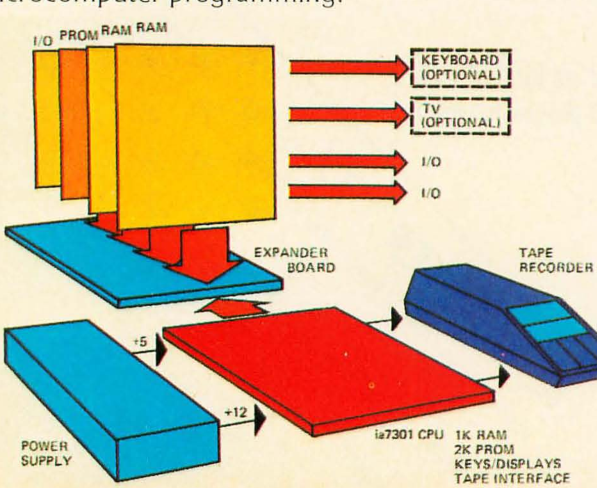
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*U.S. Patent Pending
Pong is a trademark of Atari, Inc.

Some great microcomputer features, too

The microcomputer system features a 24 pad keyboard, 8 seven segment LED readouts that display information in hexadecimal code which is far more versatile and advanced than binary or octal coded systems, and an onboard cassette tape interface for saving programs. The hexadecimal keyboard also contains 6 special mode keys which allow you to call up and change any data or instructions in the 8080 registers or in the system's RAM memory. Likewise programs can be executed instantly or they can be stepped through one instruction at a time using the appropriate mode key, so that you learn your way around the inner workings of an entire microcomputer system.

Also the write tape and read tape mode keys have been carefully designed for accurate and convenient operation with any home cassette tape recorder that has an earphone and remote microphone jack. Two LED indicator lamps tell how long it takes to dump or reload programs from the system's memory onto tape and back again. But in the reloading cycle, if any errors have occurred such as a lost piece of data, or the volume knob is too low, the readout displays will indicate errors. This little feature prevents untold problems in debugging a reloaded program.

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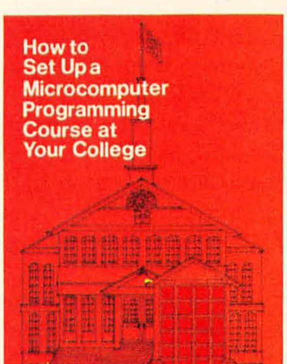


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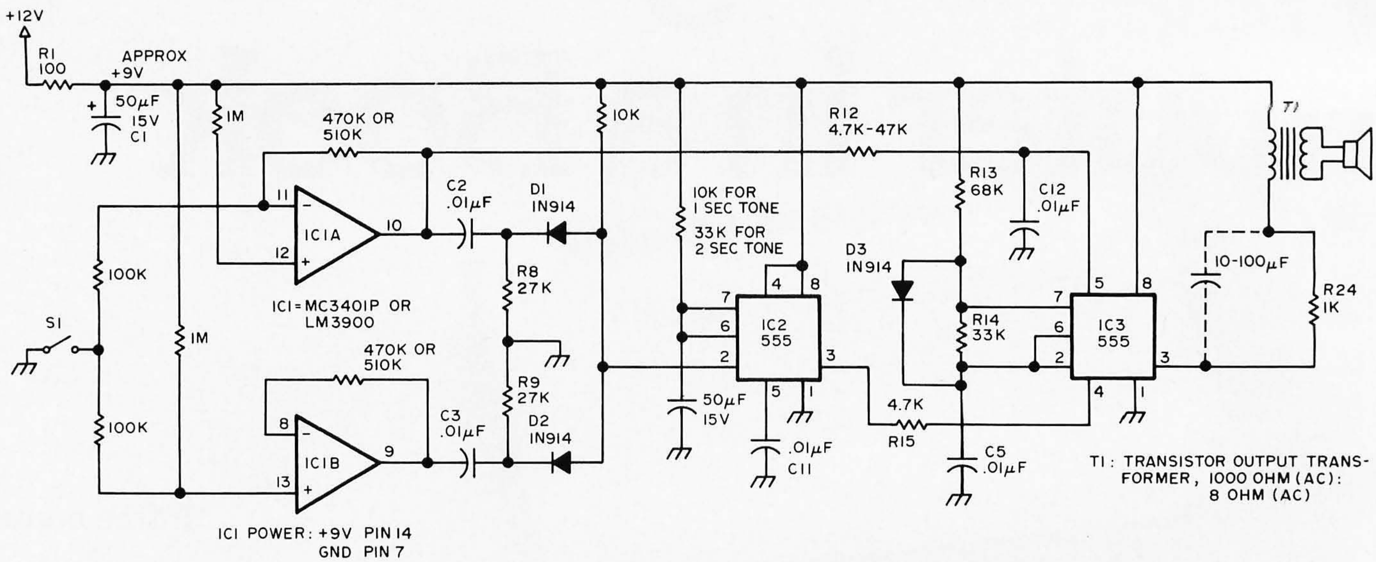


Figure 1: One way of producing audible tones on command. The input is shown as a switch, S1, at the left but could just as well be a signal derived from a single bit computer output.

of the desired tone burst. The high frequency bypasses, C11 and C12, keep the circuit from being triggered or modulated by RF noise that is present on VCC and ground.

The up and down trigger is formed from two operational amplifiers: IC1a connected as an inverting amplifier and IC1b connected as a noninverting one. Their outputs are differentiated by C2 and R8 or C3 and R9 to form a negative going spike when the input level goes up and again when it goes down. These spikes are ORed by D1 and D2 into the oneshot's trigger input.

This gives us a circuit that emits a tone whenever the input changes state. The two different tones are achieved by changing the input voltage to pin 5 of the tone generator. Connecting R12 between one of the operational amplifier's output and this pin causes the tone to shift.

The circuit worked well on 5 V. However, the volume from the speaker was less than I wanted. I had a poorly regulated 12 V available, so I filtered it with R1 and C1. You may not need them. The small loudspeaker can be connected in many ways. I had a small, inexpensive Radio Shack audio output transformer that I used with a current limiting resistor in series connected directly to pin 3 of the tone generator. Volume can be increased by putting a 10-100 μF electrolytic capacitor across R24.

Almost any operational amplifier can be used. I used a quad LM3900, so I had two sections left over. On the breadboard version I wired these together as a mixer, then fed in an audio signal from a microphone and an interesting sounding audio frequency signal from the system controller. These were eliminated in the final version, but you might have a use for similar ideas. The total cost of the complete circuit including the speaker was under $5.

But what is this system that I built? It is a complicated one compared to the 16 toggle switches it now replaces in a model railroad layout. In its final version, the system will replace approximately 600 toggle switches. More importantly, it saves many months of learning on the part of eight or ten people as they attempt to coordinate their actions in running trains on a schedule at a large model railroad club. Toggle switches are ordinarily used to direct the electrical power from each engineer's throttle to the section of track in which his train is running. The logic system takes over this job. Even after people learn which toggle switches to turn on, and when, they still forget to turn some of them off. Sooner or later this fouls everything up, sometimes in the most mysterious ways. The hardwired logic system breadboard has been working for about two years, but we are about to change over to a microprocessor system for installation in the G-C Model Railroad Club in Chicago.

Take a look at your system design. How could it be better designed for people? Is there an action required by the operator at random times? Could you use an audible interrupt? Perhaps you have a long program on a cassette and you could use an audible signal when the 10 minute loading is complete. Or perhaps you have a data link that requires attention. There are many possible uses for an audio signal to provide good human engineering.■

Cub 54,

Ralph W Burhans
Research Engineer and Lecturer
Ohio University
Electrical Engineering Dept
Athens OH 45701

What is Omega?

The Omega navigation system is a radio based method which was originally designed as an ocean locating system for shipping. It was not intended for use over the world land masses. However, the signals are free to the user no matter where he/she is located and in a sense represent another worldwide resource particularly for those who have no other radio navigation aid available. In continental USA urban areas, we have many VHF-UHF and microwave navigation aids for aircraft, so there is not much need for Omega except in remote mountain areas where line of sight propagation is restricted and the VLF-Omega is not disturbed. Omega in other parts of the world is often the only radio navigation aid available for planes and boats. Omega and other VLF systems are often used by offshore oil drilling and marine exploration crews as a means of locating their rigs or vessels particularly while in transit to and from.

The choice of frequencies and the time slot spacing is a historic matter based in part on the analog and servo mechanisms used 30 years ago. Nowadays, we have digital processing methods but some analog semiconductor receivers are still in use. Most notable

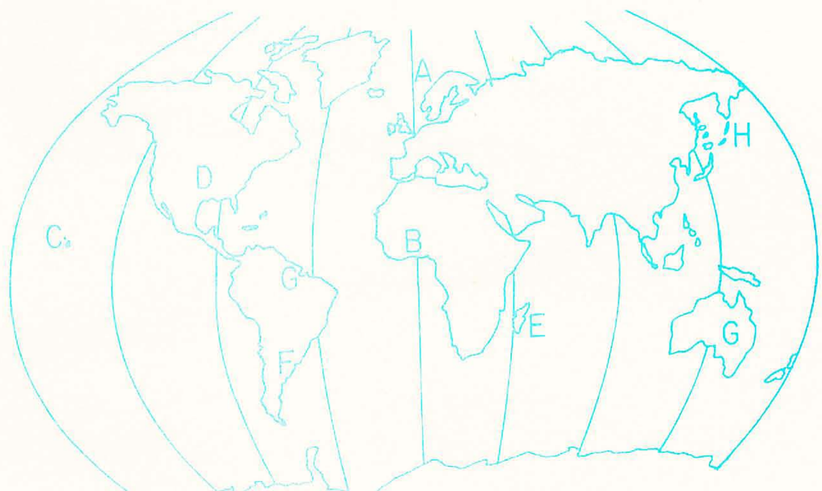


Figure 1: The worldwide Omega transmission network. The Omega system uses a set of eight transmission points scattered around the globe, emitting a pattern of bursts of radio frequencies on a 10 second cycle as shown in the table. Each possible pair of transmitters sets up a pattern of "lines of position" consisting of a series of hyperbolas one can find on an appropriate map. To find a position, phase differences between the various transmitters define a location on the Omega grid. The microprocessor control of Mini-O enables the experimenter to take advantage of Omega for shipboard or aerial navigation.

Start ← 10 seconds → Start → etc

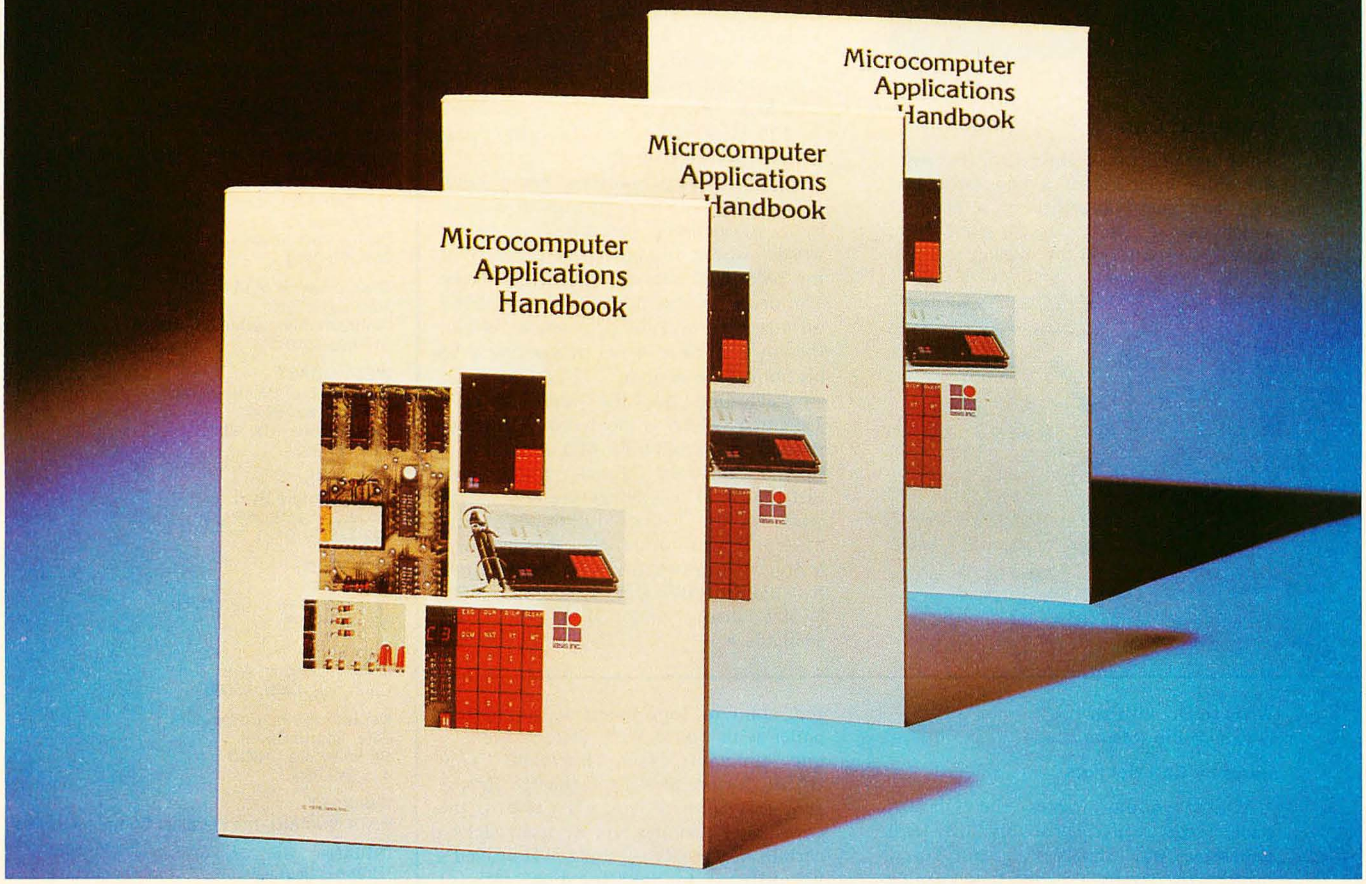
.2 sec

Stations	0.9	1.0	1.1	1.2	1.1	0.9	1.2	1.0	0.9
Norway (A)	10.2	13.6	11.33						10.2
Liberia (B)		10.2	13.6	11.33					
Hawaii (C)			10.2	13.6	11.33				
North Dakota (D)				10.2	13.6	11.33			
La Reunion Island (E)					10.2	13.6	11.33		
Argentina (F)						10.2	13.6	11.33	
Australia-(Trinidad)(G)	11.33						10.2	13.6	11.33
Japan (H)	13.6	11.33						10.2	13.6

frequency in kHz

time's arrow →

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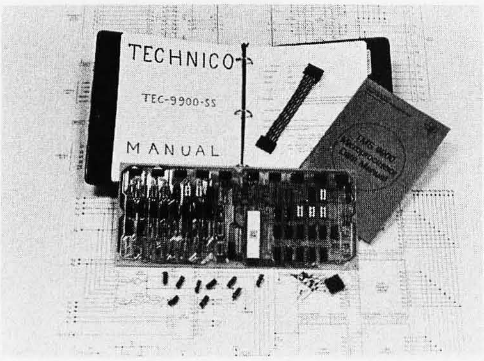
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What's New?

It's Here at Last

It usually takes some time between the announcement of a new processor chip and the availability of a product which uses it. Well, for the first time, there is a product on the market at a low price which uses the Texas Instruments 9900 processor. The product is made by Technico Inc, Columbia MD, and is a single board computer measuring 7 by 16 inches (18 cm by 41 cm) and containing the following logical characteristics:

- TMS-9900 processor
- monitor with 13 commands implemented
- on board programmer for 2708 UV erasable PROMs
- 125 page manual on the system plus wall chart schematic



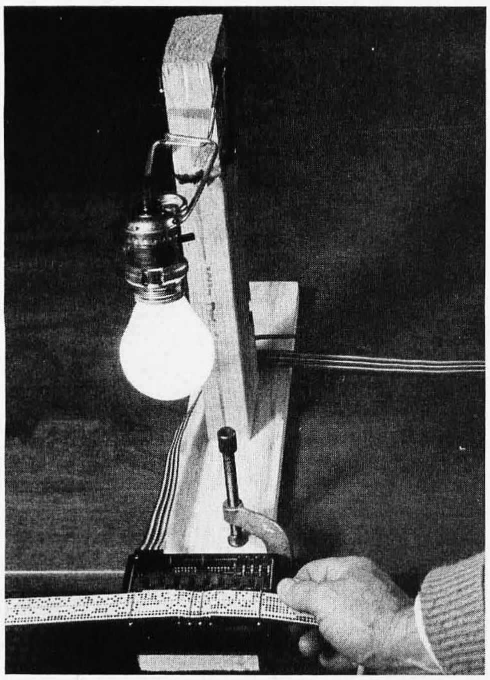
The product is a processor board only, so the user will have to provide n 8 bit bytes of memory (organized as 16 bit words) where n is up to the capacity of the TMS-9900 address space, 64 K bytes. The price for this processor board, $269 unassembled or $369, is probably one of the lowest priced ways of starting a 16 bit homebrew system.

According to the news release, Technico (which is located at 9130 Red Branch Rd, Columbia MD 21045) is a fully franchised Texas Instruments distributor. The engineering and design work for the TMS-9900 "Super Starter System" was done by Rosse Corp, Vienna VA. Information can be obtained by dialing toll free 1-800-638-2893. Dealer prices and OEM prices are available.■

What to Do with an Oliver Audio Reader . . .

notes by Carl Helmers

Oliver Audio makes the OP-80A paper tape reader, probably the least expensive way short of a homebrew project to obtain a paper tape reading facility. BYTE purchased one of these readers in order to be able to decode occasional strange letters to the editor that come on long sheets of very narrow paper with holes. Well, after loading in one program (Tom Pittman's Tiny BASIC for the 6800) and thereby debugging this form of input, I came to the conclusion that the box by itself lacks a certain degree of "solidness." It proved a bit difficult to hold the box, and for yellow paper tape the light levels proved to be critical, due to the translucent nature of the paper. So to provide a solid mounting, and a fixed but adjustable support for a lamp, I went to the woodshop, got out my saber saw, sliced up a random piece of 1 by 4 pine, used two 8 pound nails to attach a random piece of 2 by 4 vertically, then clamped the whole assembly to my bench. This photo, taken by Ed Crabtree at his studio, shows the result, using a sample of tape from a program submitted to BYTE. (Observant readers with an OP-80A and a critical eye will note one flaw in the photograph as shown here . . .)



The OP-80A was mounted on the pine board by punching two holes in its back plate with a Roper-Whitney 5J punch (a hand tool available from industrial supply sources). Two screws were then used to hold it to the board, tightening to a point where the plate was still loose with a clearance to the board slightly under the thickness of the case's interlocking groove edge. Then, when the main part of the case is slid onto the plate, the bottom of the case is tightly held against the board. The final assembly step of securing the front side of the case with screws can then be performed.■

Where Are You?

(Or How to Navigate Using Mini-O)

is the classic TRACOR Model 599 Omega receiver which has precision analog sample and hold phase locked loops with a 100 kHz reference clock. A few of these have even appeared on the surplus market.

Prof J A Pierce of the Harvard University Crufts Laboratory is the inventor of Omega. He chose frequencies and spacings based on simple number ratios. For example, 10.2, 11.33, and 13.6 are in the numerical ratios of 30 – 36 – 40, and can all be generated by integer division from a common 408 kHz clock frequency – thus 408/40 = 10.2, 408/36 = 11.33, and 408/30 = 13.6. These gear ratios and decade multiples were important considerations in Pierce's ideas because of the widespread use of mechanical servomechanisms at the time.

In the presently implemented version of Omega navigation, eight radio transmitters operate in the very low frequency (VLF) range of 10 to 14 kHz. Each station transmits a very stable frequency in such a way that a phase measurement of one station with respect to another can be made in a receiver which uses a suitable reference clock oscillator. Figure 1 shows the locations of the several Omega network stations currently in operation around the world. By measuring the phase difference between two or more pairs of stations, so-called "lines of position" may be generated. The intersection of two lines of position can be used to estimate the receiver position. The lines of position are hyperbolas which look like a skewed coordinate grid when plotted on a local area map such as in figure 2. Computed tables, charts, and diurnal (day-night) corrections are published on a worldwide basis by the US Defense Mapping Agency. The grid is very stable when the proper corrections are applied. The lowest frequency of 10.2 kHz results in a "lane" spacing of the lines of position of about 8 miles when measured on the great circle baseline connecting the two stations. Longer spacings are found, as

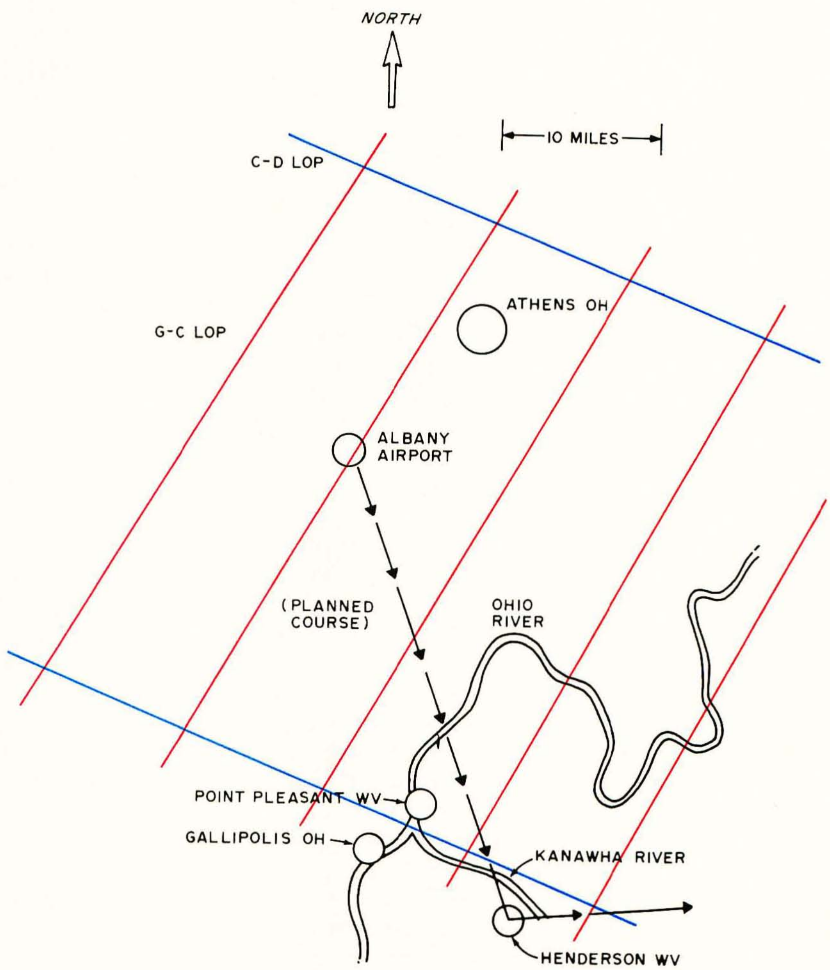


Figure 2: The intersection of "lines of position" from two Omega station pairs is depicted in this map section near the author's location in Athens OH. The picture is drawn with north at the top. The lines of position from the Hawaii (C) and Trinidad (G) station pair run from the southwest corner to the northeast corner of this local map. The lines of position from the Hawaii (C) and North Dakota (D) station pair run from the northwest to southeast in this local map. Together, these sets of lines form a local Omega coordinate grid, which can be used while navigating a planned air trip from Albany Airport OH to Henderson WV as shown by the dashed line. To use Omega, maps or tables supplied by the US Coast Guard are a virtual necessity.

would be expected, for the extreme edges of the hyperbolic contours.

In practice the usual Omega receiver works by measuring the phase between each station and a local clock reference. Phase differences are then obtained by subtracting these readings for selected station pairs. The phase differences convert directly to relative position and distance readings on a map. In Omega jargon, a centicycle is 1/100th of a cycle and directly convertible to 1/100th of a lane, called a centilane. One lane represents a 360° phase difference or equivalent to a one cycle change in the phase as used in this hyperbolic mode of navigation. Thus a navigator in a boat or aircraft can plot his or her course on a map relative to the Omega lines of position grid, and observe the crossings of these lines, called lane changes, as he proceeds to move along this course as in figure 2. The time it takes to cross a lane can be converted with simple arithmetic and trigonometry into a direct estimate of the aircraft or boat velocity. The position of the vehicle with respect to the Omega grid can be estimated by measuring the lane crossing points for two or more lines of position. A continuous measure of relative velocity and position between lanes can be obtained by eye, sampled every 10 seconds, by observing a strip chart record of two station pairs chosen for the best grid geometry relative to the receiver's current position.

The Omega system has eight stations throughout the world. Signals may be received up to 8000 nautical miles (about 14,800 km). In theory at least three of the Omega stations can be received any place on earth. The system is synchronized with atomic clocks at each station. In 1976, the time for the start of the 10 second sequence of figure 1 was set so that station A in Norway will start its cycle about 5 seconds before the least significant digit of universal time is zero, or station D will start its sequence when the least significant digit of universal time is zero. (Universal time is the current version of what used to be called Greenwich Mean Time, an international time standard, formerly derived from astronomical observation, now derived from atomic clocks.) For an observer in any of the standard time zones, where local time is "n" hours removed from universal time, whenever the local time is xx:xx:x5 he or she would find the beginning of the sequence for station A, with a burst of 10.2 kHz lasting 1.0 seconds. Incidentally, an Omega receiver can also operate as a time reference source for checking clocks since a single Omega station "ticks" at a 10 second rate, when measured on a single frequency such as 10.2 kHz. In the most elementary Omega monitor receiver the amplitude of the "tick" can become a direct check on time. However, because of the atmospheric noise and the rise time limitations of both the transmitter and receiver, it is not possible to obtain precise timing by measuring signal amplitudes. What is possible is the measurement of the phase of the Omega carrier with respect to a local reference oscillator, after the station turns on. Stations are transmitting for 0.9 to 1.2 second intervals with a gap of 0.2 seconds between each transmission. The gap insures that there is absolutely no overlap regardless of how far away the observer is from a particular transmitter.

An "Omega Users Handbook" is being prepared by the US Coast Guard Omega Navigation System Operations Detail (USCG ONSOD), and will be available shortly. *[Write US Coast Guard Headquarters, (G-ONSOD/43), 2100 Second St SW, Washington DC 20590.]* ONSOD also supplies a daily Omega status report on a taped message which can be heard by dialing the phone numbers (202) 245-0298, Washington DC, or (808) 235-2181, Hawaii. The National Bureau of Standards station WWV broadcasts an Omega status message at 16 minutes past the hour within a 42 second time slot, on the shortwave frequencies of 2.5, 5, 10, 15, and 20 MHz.

Omega has been in experimental development for 30 years and has just recently become operational. Most receivers in present use are expensive, in the $5 k to $50 k class. As yet there is a lack of worldwide demand for lowcost sets, mainly because hardly anyone has heard about Omega. It is possible to receive Omega signals with relatively simple hardware involving a parts cost of $100 or so, including a reference clock oscillator, sequence timer, and interface for phase measurements with a microprocessor system. A complete hardwired digital sensor processor can be built for under $500 in parts including data display on a strip chart recorder.

The advent of lowcost microprocessors and all the digital interfacing hardware alternatives is an obvious choice for Omega receiver systems. Commercial Omega receivers are starting to use these methods although they still command a high price ($11,000) because of the low volume of production. I wrote this article in the interest of reducing this cost and complexity problem to the bare essentials for the do-it-yourself electronics buff. There are many possible methods to consider. At our lab we have chosen what we believe to be the simplest methods, not necessarily the best.



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As others become aware of Omega, it is very likely that further improvements and simplifications can be achieved.

VLF (Very Low Frequencies)

Frequencies in the 10 kHz to 20 kHz region propagate in a mode where the earth and its ionosphere form a cavity which acts as a spherically symmetric waveguide. At the low end of the range the ionosphere is only about 2 wavelengths (60 km) high and single mode transmissions may be received over very long ranges.

For the simplest Omega propagation monitor or computerized do-it-yourself navigation aid, the single channel frequency of 10.2 kHz is desirable. The higher frequency of 13.6 kHz will give somewhat more signal strength but more problems are created due to multimode transmissions. The ideal VLF frequencies which minimize diurnal changes in the received phase would be about 11.9 kHz for daytime paths and 12.2 kHz for nighttime. It is interesting to note here that the USSR has an "Omega like" navigation system which uses 11.905 kHz, 12.649 kHz and 14.881 kHz. The reason that these VLF methods use several different frequencies is to resolve the lane ambiguity to much greater than 8 nautical miles for the 10.2 kHz case. Thus a difference frequency like 3.4 kHz can be generated from 13.6 − 10.2 with a suitable complex receiver and processor system. For Omega, the 3.4 kHz would result in a 24 mile lane. However, a single frequency receiver can be used to provide correction on position when good dead-reckoning data is available from the navigator who keeps track of his/her course direction and independently estimates velocity (or guesses it from wind drift, pitometer readings, air speed-temperature corrections, etc). Thus a single Omega frequency used completely without reference to anything else can only resolve position-velocity to within one Omega lines of position grid "square," and the problem is to decide which of many possible grid locations (separated by 8 mile intervals at 10.2 kHz) is the correct one. Of course the navigator should know from where he started and his destination, so that at least the initial conditions for navigation are available. Then the Omega receiver along with dead-reckoning data can be combined to give a better estimate of the true position after starting along a known course line. In effect the Omega receiver can give an independent estimate of the vehicle velocity and the microprocessor or even the pocket calculator can help in manipulating the numbers involved in the computations.

Because of atmospheric noise and other uncertainties in the propagation caused by sunspots or polar cap absorption, the typical Omega receiver resolves position to something like ± 1 nautical mile (1.8 km) when the diurnal correction tables are applied. For local area users, starting from a known point, a single frequency receiver should be able to resolve Omega positions to within ± ¼ mile (0.3 km) in the absence of gross interference to the received signals, over a short duration mission (one hour or so) that is not near sunrise or sunset.

Another technique for improving the precision of Omega is to compare the navigator's received phase with a known ground station's received phase over a 100 mile radius for differential corrections. The local ground monitor has to transmit an almost continuous data stream of its Omega readings to insure that some short duration propagation anomalies did not cause a "lane jump" or some other error. The ground data is transmitted to the remote user via another radio link. Differential corrected monitor systems have been used to determine the position of weather balloons by having the Omega signals modulate a UHF carrier frequency retransmitting the data to ground stations where the data is processed.

As with most radio communications systems, Omega suffers from the usual signal-to-noise problems for the ultimate resolution. The general atmospheric noise level caused by thundershowers on a worldwide basis creates field strengths of 10 to 100 μV per meter in a 30 Hz bandwidth at the Omega receiver antenna. The lowest detectable Omega signals may be only 10 μV, often buried in 100 μV of noise. Local thundershowers and 60 Hz harmonic interference also plague Omega users. Wire antennas are best for picking up strongest signals, but also respond just as well to all the noise. A loop antenna can discriminate against some noise due to directional nulls but suffers from the problem that the phase of the Omega station signal reverses when the loop is rotated through 180°. A much more complex receiver system is required when using a loop antenna system.

Some Fine Points on the Omega System

The suggested range for usable reception of Omega signals is 600 to 6000 nautical miles (1,000 to 10,000 km) from the transmitter. When a receiver is close to a station the phase measurement to that station will be in error because of multiple mode propagation. Another problem near a transmitter is that the receiver may need to reject the unwanted signal from the local transmitter in order to receive a desired signal of some

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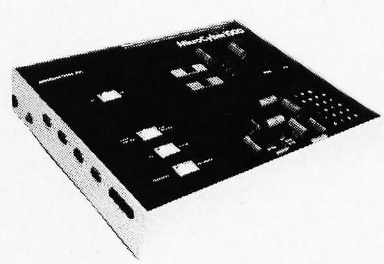
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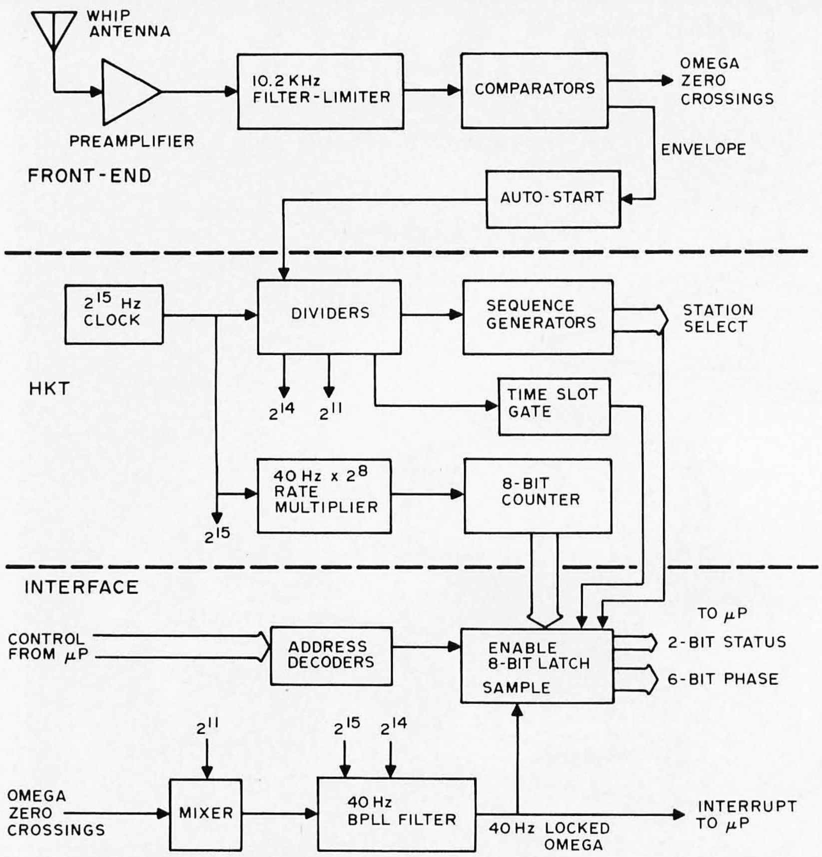


Figure 3: Block diagram of the Mini-O system. The system is shown here in outline; details of the hardware are found in part 2 of this article. The microprocessor is a key element in the processing of Omega information, making it possible to save thousands of dollars relative to the least expensive commercial equipment.

other transmitter on a different frequency. Thus the skirt selectivity or adjacent channel rejection capability of the receiver is of some importance. An example would be North Dakota transmitting on 11.333 kHz when trying to receive Argentina on 10.200 kHz, where the 11.333 signal might get into the 10.200 front end.

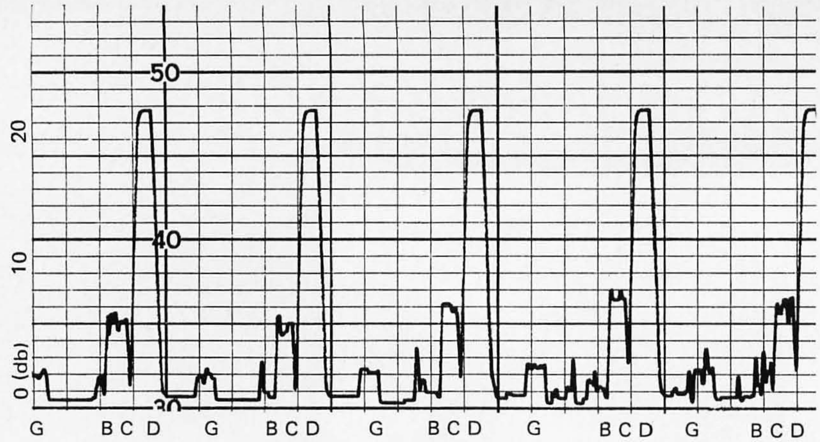
In the USA many observers will have trouble receiving the A channel from Norway. The path of the propagation over the Greenland icecap is severely attenuated. The ice acts like an absorber (similar to a giant size carbon wedge as often used in microwave waveguide attenuators). Omega is also affected by sunspot activity or any radiation that disturbs large blobs of the ionosphere.

Omega signals may be received underwater. The "skin depth" of sea water at 10 kHz is appreciable so a submarine or underwater explorer with a trailing wire antenna can in theory use Omega for navigation purposes. Reception in airborne systems is usually quite good except for a phenomenon known as precipitation static when charged rain or snow particles hit the antenna in sufficient quantity to obliterate the signals. Loop antennas tend to reject this type of interference and are found in many commercial or military airborne receivers.

The choice of the spacings between channels and length of transmissions, varying from 0.9 to 1.2 seconds in 0.1 second increments, was made so that an observer might use the station on times to uniquely determine which combinations of stations are being received. This is a nonredundant sequence of time intervals. Nowadays we can also do this with an automatic synchronization software routine which first has to monitor a hundred or so seconds of Omega frames and decide where the usable signals are, before starting up a sequence generator at some point in the frame. However, a much simpler synchronization method may be used when a strong station signal is available.

For North American users (Mexico, USA and Canada) the D channel at North Dakota will usually provide a positive identification based on signal amplitude only without any fancy software required. This saves us a lot of trouble, particularly in the early stages of experimenting with Omega sensor systems. Observers in other parts of the world, for example in Europe, might use the A station at Norway for an easy way of identifying where the Omega system is synchronized to the local reference. Similarly the African nations can use Liberia or LaReunion Island, South America can use Argentina, and the Northern Pacific Ocean area can use either Japan or Hawaii. Temporarily, G channel is assigned to Trinidad, but this will be moved to the South Pacific area at some future time.

A few words about the concept of frequency offset are needed to help in understanding Omega systems. We discuss the offset of one clock with respect to another in terms of how many cycles they are apart. Thus two 1 MHz oscillators turned one Hertz apart in frequency might be said to be offset from each other by 1×10^{-6} which means that one clock will "beat" with the other at a rate of 1 cycle every million cycles with respect to whichever one we call the standard. We can talk about an Omega clock which appears to be changing (drifting) 1 lane (1 cycle) in, say, 60 seconds. The offset here would be expressed as the time of one Omega cycle divided by the time taken to change one cycle or: $1/10200/60$ seconds = $9.8 \times 10^{-5}/6 \times 10^{1} = 1.63 \times 10^{-6}$. Here the clock itself appears to be giving a one lane change every 60 seconds. However if we use this clock with respect to Omega stations C



Relative Signal Levels ← 10 sec →
0800 AM EST 4/11/76

Figure 4: Signal envelope from the Mini-O receiver at 10.2 kHz. This is a photo reproduction of a strip chart recording made from data taken at 8:00 AM EST on April 11 1976.

and D which are only about 1 second apart, *and*, we subtract the two readings (D vs clock from C vs clock), then only about 1 second elapsed between the measurements. The error in the measurement is thus about 1/60th of a lane which is negligible. Furthermore, this is a constant error which does not change appreciably with time or from station to station.

Still another factor involved here is the fact that the vehicle may be moving with respect to the fixed positions of the Omega stations. This is, of course, what we are trying to measure; that is, how fast are we moving with respect to a particular station pair? The Omega receiver output gives a reading or plot on a strip chart recorder which is the line of position desired. The rate at which this reading changes or moves across the chart with a repeat at every "lane change" in a sawtooth fashion, is the basic data of the Omega system. Two such records specify where the receiver is located provided we knew from where we started and did not loose count of the number of lane changes (sawteeth lane count) made. Many marine navigators like to use the filtered Omega lines of position phase differences in this manner because it gives them a rapid idea of where they have been and how fast they are going in a graphical display as opposed to reading out numbers on a digital display. Thus most digital Omega processors can also provide digital to analog conversion outputs which can be programmed for lines of position data, or with more sophistication, even plot a course with a "bug" on an X-Y moving map display. But a boat is by nature slow.

In contrast, the general aviation pilot doesn't have time to watch these interesting displays and is usually supplied with data in the form of a computed miles to go to some waypoint and a heading error indicator which is obtained from some kind of digital data processor. Simplified software for this is in the development stage at the present time. Most of the software for the filtered lines of position display has been worked out and will be detailed as part of this series of articles on Mini-O.

There are a great many problems for a microprocessor experimenter to study. In particular, the output of data in coordinate systems like latitude and longitude instead of Omega lines of position; the correction of lines of position estimates with diurnal lookup tables or ionosphere models; and the use of multiple frequency Omega channels, are fruitful areas for some simplified software data reduction methods.

An area of interest using microprocessor software techniques is that of providing velocity aiding loops which estimate the rate of change of the received phase and increment the memory ahead or predict where the phase should be for the next time slot. In a moving vehicle using only three stations, we can directly track at general aviation velocities (< 150 knots or 277 kph). However, at jet velocities a more sophisticated mathematical technique called a second order loop is of some value. A second order loop also improves the signal-to-noise because it tends to correct for clock error although the clock drift is not easily determined independent of the vehicle motion when using only three stations on a single frequency. With four or more stations being received or when using more than one frequency in several different receiver front ends, the clock error may be estimated and the system used in the direct ranging mode. This doubles the lane distances to 16 miles measured as concentric circles surrounding each transmitter instead of the hyperbolic station pair difference mode. These methods require more software, and about double the complexity of the receiver front end.

In the longer range future we might contemplate that BYTE readers could exchange information on "DX" reception of Omega signals at very long ranges such as from Japan or LaReunion Island for USA observers, using super software tracking loops able to dig signals out of a lot of interfering noise. Software methods of improving the reception for weak signals would be of value for the future utility of Omega.

Hardware areas also need some improve-



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ment. In particular someone needs to invent a single op amp (single +5 V power supply using one section of a quad) noise editor that will blank out wide band noise pulses without generating transients driving the narrow band filters. Noise blankers are a well known art, but what this world really needs is a simple one that does not double the front end complexity of the present Mini-O system.

Omega Sensors

All Omega receivers involve some analog radio frequency circuitry in the front end to amplify the microvolt signal levels up to values sufficient to operate digital processing systems. It is highly advantageous to use a lot of sequential narrowband filtering to improve the resolution of the resulting square wave edges. A typical Omega receiver will have a preamplifier, a set of narrow band filters, some type of limiter, and finally a comparator to generate edges for phase processing. Preprocessing bandwidths in the 30 to 100 Hz range are found in most commercial systems. The advent of quartz tuning forks and mechanical filters operating in the 10 kHz region makes it possible to have a relatively simple system with 4 to 15 Hz bandwidth. Very narrow radio fre-

GLOSSARY OF OMEGA TERMINOLOGY

This is terminology frequently found in Omega literature, some of which is used in these articles. Readers will find this glossary a useful guide to detailed study of Omega navigation.

Frame — One complete 10 second Omega sequence of transmissions.

Time Slot — The time within a frame when one station transmits on a single frequency according to the table in figure 1; simultaneously several other stations will be transmitting on the other frequencies in the same time slot.

Lane — Spacing between adjacent LOPs which are 360° apart electrically, but measured over the earth surface usually in nautical miles. Note that this distance will vary from 8 miles in the center of the hyperbolic pattern to 25 miles or so at the extreme baseline extensions of the station pair in question.

Centilane — One hundredth of a lane (1/100). (Abbreviated CEL.)

Cycle — Phase difference of 360° between two transmitters as measured at the receiver.

Centicycle — One hundredth of a cycle (1/100). (Abbreviated CEC.)

Line of position — Path of constant phase difference (usually at 0° or 360°) between two transmitters as measured over the earth surface. (Abbreviated LOP in literature.)

Epoch of A — Start time of the A transmitter (NORWAY station on 10.2 kHz) with respect to UTC (Universal Coordinated Time as referenced to atomic cesium clock time).

Difference Omega — Use of two or more frequency channels to generate longer range LOPs as 13.6 − 10.2 = 3.4 kHz.

Differential Omega — Corrected line of position measurements using a nearby fixed ground reference receiver.

Composite Omega — Mathematical weighting of received phase on 10.2, 11.33, and 13.6 to generate pseudo frequencies such as 11.9 or 12.2 kHz for reducing effects of diurnal changes.

Diurnal — Day to night changes in the position of particular station pair lines of position as measured over the earth surface.

Offset — Frequency difference between two clocks usually expressed in fractional cycles where cycles are defined in terms of UTC seconds (Hz), may be expressed as $\Delta f/f$ or $\Delta t/t$.

PCA — Polar cap absorption associated with solar radiation which causes Northern Lights type of display — may last for hours or days and disturb signals which propagate over the polar regions.

SID — Sudden ionosphere disturbance, changes in the height and density of the ionosphere caused by showers of solar radiation particles associated with sun spots.

Prop — Propagation of VLF signals as it refers to Omega, such as "prop error."

Precip or P-static — Precipitation static due to charged water, snow, ice, fog, rain, clouds, striking conductive surfaces and antennas. Most pronounced in aircraft "E-field" antenna systems, but also observed in marine and ground monitors, particularly during very cold dry blowing snow, or sudden rain showers underneath thunderheads.

PPC — Predicted propagation corrections as obtained from tables, or computer programs built in to Omega navigation systems.

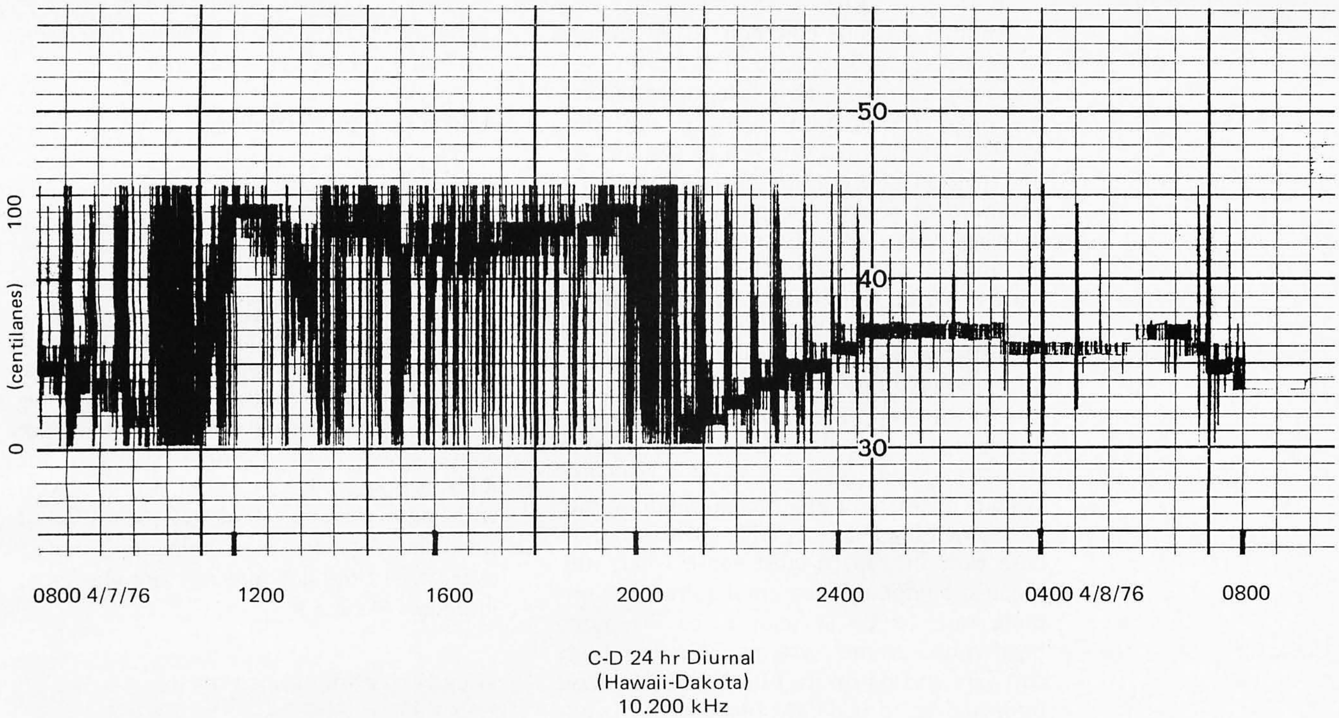


Figure 5: A 24 hour record of raw data received with one of the first test rigs of the Mini-O design. During the daylight hours, considerable 60 Hz interference was noted. This results from the fact that noisy electrical machinery or high power SCR or TRIAC controls connected to the local AC power system of the laboratory generate significant amounts of the 170th harmonic of 60 Hz, 10.2 kHz. This recording was made using a 4 bit precision for phase differences between the C and D station pair of the Omega system on April 8 1976. A total of 8640 consecutive measurements were made during the day, once every 10 seconds. The results were recorded on a Heathkit chart recorder as they were measured with a 200 minutes per inch chart drive speed.

quency bandwidths like 0.5 Hz cannot be used because the filter bandwidth is less than the "on time" of the signal. Other types of filters involve ceramic and mechanical magneto-restriction devices. Another method that has sometimes been used is the superheterodyne receiver where a local oscillator is mixed with the Omega signal to generate an intermediate frequency such as 1 kHz or lower where the bandwidth of the intermediate frequency is inherently narrower than the incoming signal amplifiers.

The receiver local oscillator or reference oscillator used for phase comparison must have good stability and a frequency offset of less than 5×10^{-6} to insure that the phase difference over a several second gap does not drift more than a few centicycles. Quartz crystal oscillators can provide this. Most receivers use what is called a TCXO (temperature compensated crystal oscillator) which can be set to an offset of 1×10^{-7} and will maintain this low offset within 1×10^{-6} over a reasonable operating temperature range (the short term stability over several hours is usually much better). The low frequency quartz oscillators used in digital watches (2^{15} Hz) can provide better than 1 second per week (about 5×10^{-6}) low offset capability when treated with some care. The most expensive Omega receivers sometimes use an atomic clock reference and can operate in the direct ranging mode, comparing each station to the atomic clock without subtracting station pair differences.

The receiver clock system (housekeeping timer) should provide some means of generating the desired Omega sequence intervals and a suitable reference for the phase comparison. It is convenient to choose a crystal oscillator frequency which has some direct and simple relation to the Omega frequency desired. A TCXO clock on 2.6112 MHz is often used ($2^8 \times 10200$ Hz). Other receivers may use a standard 5 MHz reference and a complex frequency synthesizer to provide equivalent references. If we think in terms of binary systems, it is possible to devise intermediate frequency types of digital processors which use 2^n Hz as the basic reference or BCD equivalents like 1 kHz, 100 Hz, 10 Hz, 1 Hz and 0.1 Hz. The Mini-O system to be described uses a 2^{15} Hz clock to provide all the reference frequencies including the Omega sequence timing rate.

Another feature common to all Omega receiver systems is some form of multiplexed phase locked or recursive filtering applied to the phase information following the comparator. Digital hardware sensor systems are one method where a suitable clock system is advanced or retarded in phase by adding or deleting pulses to a countdown chain. An up-down counter system can also be used with a digital comparator. Software based digital filters have been devised which are basically recursive low pass filters operating at a relatively low sample rate. The sampling rate of the original edges is controlled by the analog radio frequency bandwidth used in the front end. Thus a 30 Hz bandwidth system might require a digital sampling rate of something like 100 Hz for optimum detection in the Nyquist sense where the Nyquist Sampling Theorem requires the sampling rate to be at least twice the input bandwidth. Some systems combine both software and hardware filtering of the phase information to generate final output bandwidths of the information down to 0.01 Hz. With this narrow effective bandwidth, the receiver requires a long time (2 minutes) to lock up on the signals and correspondingly can hold lock through a lot of transient noise where the signal drops out momentarily. These digital systems are inherently sample and hold types where a shift register, counter, or latch holds the data for each Omega time slot in a multiplexed operation.

Current research effort among microprocessor Omega researchers is involved with the development of software based sampling systems at a suitable low interrupt rate where the microprocessor itself becomes the equivalent of the voltage controlled oscillator as it is used in analog phase locked loops. These are still in the development stage in our laboratory.

Mini-O Receiver Concept

The simplified Omega receiver methods which have been used for a basic digital interface are shown in block form in figure 3. This consists of a short whip antenna, a radio frequency preamplifier, a 10.2 kHz narrow band filter and limiter, zero crossing and amplitude gate detectors, clock and housekeeping timer, and finally a binary sampled phase output module. The output consists of 4 to 8 bit words which are processed after interrupts which occur at a 40 Hz rate. The master crystal clock labelled HKT in figure 3 supplies all the timing functions necessary to operate the Mini-O as an independent monitor receiver or as an interface for a microprocessor system. The modules may also be used to drive hardware digital filters or analog type signal processors depending on the user's interests.

4 Bit Raw Data Recordings

The Mini-O receiver is a digital superheterodyne design which indirectly mixes a 10240 Hz local oscillator with 10200 Hz to generate a 40 Hz intermediate frequency difference. Because the local oscillator is on the high side of the signal, the phase change of the 40 Hz intermediate frequency is reversed in direction with respect to Omega. In the first work on this system a sampling rate of 8 Hz or 40/5 was used because of convenience. By averaging 5 cycles of the 8 Hz samples, a binary count was generated with 4 bit precision. Example recordings of this raw data for measurements averaged over single time slot intervals are illustrated in figures 4 and 5.■

The second part of this series of articles by Ralph Burhans and his associates at Ohio University will follow in next month's BYTE. In part 2, you'll find details of the hardware of the Mini-O receiver, which can be built by the advanced experimenter with interests in navigation problems. Part 3 by Richard Salter follows with information on processing software.

SELECTED REFERENCES ON VLF NAVIGATION AND RELATED TOPICS

On general VLF applications:
J M Beukers, "A Review and Applications of VLF and LF Transmissions for Navigation and Tracking," *J Inst of Nav 21 No. 2,* pages 117-133, Summer 1974.

On optimum VLF frequencies:
R Grover Brown and R L VanAllen, "Three Frequency Difference Omega," *Proc Nat Aero Symp*, Inst of Nav, Warminster PA, April 27-28 1976.

On RF preamplifiers:
R W Burhans, "Single Preamplifier/Isolator Drives LF and VLF Receivers," *ELECTRONICS 48*, pages 107-108, Sept 4 1975.

On previous simple receiver designs:
R W Burhans, "Phase-Difference Method Offers Low-Cost Navigation Receivers," *ELECTRONICS 47*, pages 98-105, Sept 5 1974.

On digital concepts for Omega receivers:
R W Lilley, "Binary Processing and Display Concepts for Low-Cost Omega Receivers," *J Inst of Nav 22 No. 3*, Fall 1975.

On microcomputer-based Omega systems:
R W Lilley and R J Salter, "Simulation Analysis of a Microcomputer-Based Low-Cost Omega Navigation System," *Proc Nat Aero Symp*, Inst of Nav, Warminster PA, April 27-28 1976.

On analog amplifiers and limiters:
W G Jung, *IC Op-Amp Cookbook*, Howard W Sams Co, Indianapolis IN, 1974.

On microprocessor interfaces:
D Lancaster, *TV Typewriter Cookbook*, Howard W Sams Co, Indianapolis IN, 1976.

On applications for simple Omega receivers:
R W Burhans, "Mini-O, Simple Omega Receiver Hardware for User Education," *Proc 1st Int Omega Assoc Symp*, Washington DC, July 27-29 1976.

The POLY 88 Microcomputer System

If you are into computers or considering a system, the POLY 88 is the machine to contemplate.

HARDWARE

• Popular 8080 central processor • Single-board CPU with ROM, RAM, vectored interrupt, real time clock, single-step logic and serial I/O • Video interface card – generates video to TV monitor and provides parallel keyboard input port • Serial and cassette mini-cards plug directly into CPU with ribbon cables • Cassette • ROM monitor with powerful debugger, video software, bootstrap loader • Backplane and power supply on one board simplifies construction • Rugged 6 amp power supply • All circuit boards are high quality, double-sided with plated-through holes • System is compatible with a wide range of Altair peripherals • Minimum point to point wiring means that the POLY 88 kit can go together in three evenings!

ABOUT SOFTWARE

Software is the reason the POLY 88 was designed. The operator can proceed from higher level languages like BASIC to developing machine code with the aid of our assembler. Our BASIC is a full 8K BASIC with character and byte manipulation. Best of all, the programmer is finally free of the teletype emulation mode so the video display can be used to full advantage.

The video display provides a unique opportunity to write new types of programs and games. Characters (16 lines of 64) and graphics (48 by 128 grid) are part of the processor's memory, so the display may be altered rapidly — the entire screen written in less than 20 milliseconds.

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SYSTEM 1 — Kit includes 8080 vectored interrupt processor with real time clock, ½ K of RAM and 1K monitor on ROM: Video Terminal Interface displays 16 lines of 32 characters on a video screen and has a keyboard input port; cabinet, backplane, and power supply; complete assembly, operation and theory manual. $595.

SYSTEM 2 — System 1 plus 64 character line option and Byte/biphase cassette interface kit. $690.

SYSTEM 3 — System 2 plus 8K of RAM with BASIC and assembler programs on cassette tape. $990.

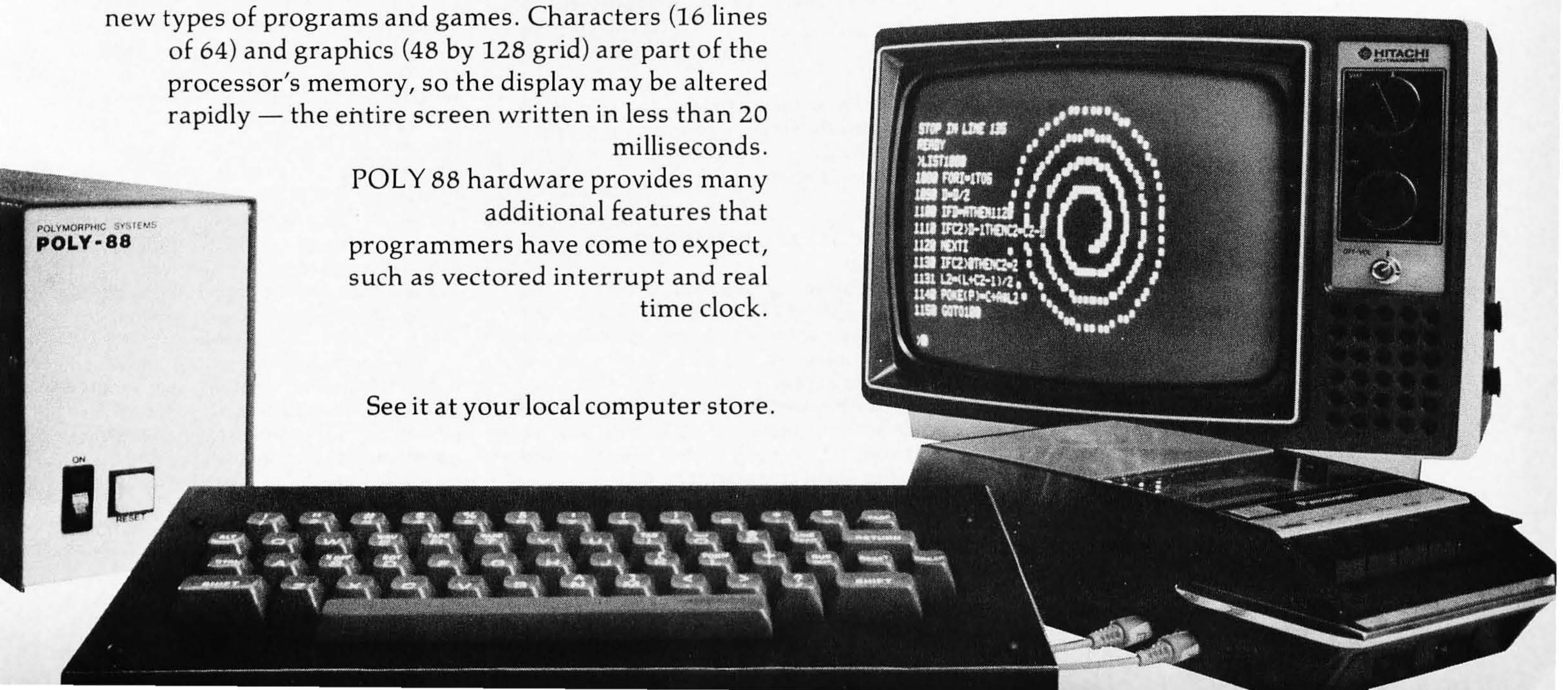
SYSTEM 4 — The complete kit. It includes system 3 *and* TV monitor, keyboard and cassette recorder with all necessary cables and connectors. $1350.

SYSTEM 7 — System 4 assembled, tested and ready to run. $1750.

ACCESSORIES — 8K RAM kit, $300. Assembled $385
POLY I/O Ideaboard, hardware prototyping kit board. $55.
Analog Interface (1 channel) kit. $145.

Prices effective until January 15, 1977. Prepaid orders shipped postpaid.

PolyMorphic Systems 737 S. Kellogg, Goleta, CA 93017
(805) 967-2351



Continued from page 11

IBM Selectric series. I would like to have some suggestions and comments on this proposed project from other readers. Any readers who can give any information on how to convert the IBM Selectric to a teleprinter will be greatly appreciated.

Ronald K S Chan
Engineer, Engineering Laboratory
Canadian General Electric Co Ltd
3-397 Reid St
Peterborough, Ontario
CANADA K9H 4G4

FLEXOWRITING

RUN

Dear Sirs,

In recent months the Friden Flexowriter has begun to turn up in numerous classified listings and surplus catalogs as a new possibility for a relatively inexpensive hard copy output device. To those contemplating purchasing one of these units, this letter stands as evidence that they can indeed be interfaced to a micro's output port without too much difficulty. This letter was typed by a model 2301 Flexowriter interfaced to my homebrew 8080-based system running Basic.

The interfacing of the 2300 series of Friden Flexowriters is similar in many respects to interfacing old Baudot-code machines, but there are many advantages to the Flexowriter. First is obviously having both upper and lower case. This plus the typewriter-type font on most models make the unit very applicable to text-editing and typing programs. Second, the Flexowriter types at a practical 12codes/sec. (The actual number of characters/sec depends on the number of case shifts necessary in the text.) Third, the standard 16-inch carriage provides more than 160 columns of output, and if you're lucky enough to get the optional 20-inch carriage, well......

There are many different Flexowriter models and many variations of each, so the prospective buyer may find the following information of help. The 2200 and 2300 series of automatic typing machines are the most applicable of the commonly available models. While like most Flexowriters, they have a non-standard 8-level code (which is very easily reduced to a 7-level code) they usually feature a standard 8-level paper tape punch and typewriter-type font. The 2304 even boasts proportional spacing and secretary-shift, which might make interfacing easier.

The 2200 series usually has a larger character set and many models have the 20-inch carriage..

While the above units usually include a mechanical tape reader and code output from the keyboard the necessary code conversions make it much more practical to use a separate ascii-encoded keyboard and optical tape reader for the system input.

In short, the Friden Flexowriter can provide a very suitable hard copy device. Certainly the price of most of them alone makes them quite attractive. I obtained two such units through rather fortunate circumstances for free. They can be interfaced to a parallel ascii port for less than $50, much less if you're a good scavenger.

Anyone contemplating, or actually attempting to interface a Flexowriter to his micro may write me at the below address and I will be glad to help in any way I can.

Sincerely,

Bob Rindfuss
2367 Yeager Rd. #115
West Lafayette, IN
47906

OK

The letter is reproduced here photographically to show the type font and demonstrate the practicality of Flexowriters.

REGARDING BAR CODES, CONTINUED

I read with great interest your article "A Proposed Standard for Publishing Binary Data in Machine Readable Form" in the November 1976 issue of BYTE. I am very much interested in the problem of publishing software in cheap and easily transmitted form. Cassette tapes require an expensive (~$100) interface as well as a not so cheap (~$3) tape. Your method requires only a piece of paper and a light pen hooked up to a single input bit of a microcomputer. The software is relatively simple, and doesn't take up that much room. (Remember, once the program has been read successfully, it can be transferred to your own cassette system, if needed.)

I am worried about one aspect of the standard that you discussed in your article. I think that *reliability* is the key issue — more important than either people, readability or density. Furthermore, this reliability should be conserved through making at least one Xerox copy. I do not know the characteristics of a Xerox machine that well, but I can conceive that they consistently either make the black bars narrower or wider. This might cause all ones to be mapped into zeros or vice versa. I think that in addition to a longitudinal parity check, there should be a parity bit on each character. This method allows single bit *correction* instead of single bit *detection*.

I have done a little experimentation with your code format 2, which seems to have the most reliability built in. It seems that 1/5 inch is probably more than necessary for the length of the bars — 1/7 inch looks good. I also think that whether the code is published in columns or rows is not so important (unless someone is planning to build page readers).

I include the first paragraph of this letter which has been coded into bar code and produced by the MIT Artificial Intelligence Laboratory Xerographic Printer. This printer has 200 dots/inch resolution, and each character is 28 dots high and 48 dots wide. All of our software is line oriented, so I have taken the liberty of making the bars vertical instead of horizontal. Since the characters use format 2, each zero is 2 black lines followed by 4 white lines and each one is 4 black lines followed by 2 white lines. (The lines are only 1/200 inch wide, so that they merge together into bars.) Using this format, we can put 28 characters on a 7 inch line, 66 lines on a 10 inch page. This gives a total of 1848 bytes/page. No synchronization or parity characters have been used, although they could easily be added.

Henry G Baker Jr
MIT Laboratory for Computer Science
545 Technology Sq
Cambridge MA 02139

This is the complete text of a letter printed in bar code form in last month's BYTE. See January BYTE for the bar code text referenced.

APL INTEREST?

Inspired by the APL article in the November BYTE, I would like to get together with some other people who have access to an APL system or are looking ahead to their own microprocessor based APL system and would like to build or modify a CRT or dot matrix impact terminal to display the APL/ASCII character set.

I have some ideas which I will share on how to incorporate overstrike capability in a CRT terminal inexpensively; but the character generator is the problem. APL character generator ROMs are nearly impossible to acquire and I would like to have one manufactured.

If anyone is interested please send me your name and address along with any comments you may have. For example, would you prefer 5 by 7 (similar to the APL Decwriter) or 7 by 9 character matrix? If I perceive sufficient interest I will have the chip encoded and send you information. I expect cost per chip to be about $30.

Phillip Apley
Hampshire College Box 9
Amherst MA 01002

DELIVERY COMMENTS

In December 76 BYTE you included a product review by D Anderson of our VDM-1 Video Display Module. He did a good job on the technical side; however, I am pleased to update the 60 day delivery time he referred to. We are now delivering the VDM-1 and most of our other products FORTY EIGHT HOURS after receipt of order when a money order or certified funds are included with order.

Terry M Holmes
General Manager
Processor Technology Corp
6200 Hollis St
Emeryville CA 94608

IDENTITY CRISIS: ARE WE NERDS?

In the letters section of the October 1976 issue of BYTE, Bryan Patterson posed the question of what computer hobbyists should call themselves. Your preference for the term "hacker" leaves much to be desired, as most computer professionals could legitimately claim this term, particularly those who specialize in software development at other people's expense.

In spite of over 25 years of commercial application, computer system development is still largely an undisciplined form of self-expression, using ad hoc design methods, usually resulting in late and over budget delivery of unreliable products. Recent developments in software engineering are largely scorned or ignored by the "artists" of the profession. Standards, usually a sign of stability and maturity of a profession, are largely ignored as being a damper on the free spirit of creativity. Judging by the practices and results achieved by the professionals in the computer field, I would say the term "hacker" belongs to them.

The computer hobbyist, on the other hand, is working with his own money and is his own customer. Some professionals are also hobbyists, but it is my observation that more planning and careful design goes into their personal systems than in their professional activities. Some of this is due to severe limitations on their personal resources, to be sure,

and such limitations always seem so obvious. The rapid adoption of such things as the KC cassette standard and the Altair bus (as a de facto standard) are real signs of maturity. The free exchange of information, construction tips, programs, etc, by hobbyists, as opposed to the publications of thesis papers on the professional level, is much more practical in an engineering sense.

I would not claim that the hobby computer field is not subject to muddling, but it has a "can do" spirit to it.

The computer hobbyist seems to be interested in the novelty, education, recreation and delight offered by the small programmable systems. An acronym composed of the first letters of those attributes of amateur computing spells "NERD," which might be a term suitable for the computer hobbyist. Next time, Mr Patterson, you can say, "Hi, I'm a computer nerd!"

Dick Curtis
4741 Newlons Dr E
Murrysville PA 15668

DIRECT BINARY?

I was reading your article in the November BYTE (issue #15) entitled "A Proposed Standard for Publishing Binary Data in Machine Readable Form." I thought it was a very good idea and I had considered it myself as a good way to store data in bulk and an easy way not to have to load in by hand programs that you see in magazines. However, I think that there is an easier format than the ones proposed in your article. The following format is similar, but takes up less space and has a consistent bit length:

```
V1←[XXXXXXXXXX
V0←[
V1←[XXXXXXXXXX
V1←[XXXXXXXXXX
V1←[XXXXXXXXXX
V0←[
V0←[
   .
   .
   .
        ETC.
```

Where Xs represent a solid black line with no gap between lines and blanks represent an area with no ink at all.

I hope you will consider using the above format as it could simplify it greatly and also save some paper.

Wayne Loofbourrow
815 Standish Av
Westfield NJ 07090

This method suffers from the problem that it is not self-clocking. A format for bar codes, to be usable, must be self-clocking, which virtually requires some redundancy in the encoding.

I NEED EASY COMPUTERS!

Right now all I have going for me is a desire to use a computer, a little knowledge I have gained of computers from books, and a subscription to BYTE. Even with the dropping prices of microcomputer hardware, being a student, I still cannot afford a computer. How about an article on building your own microcomputer, using easily available parts and easy construction techniques, with provisions for expansion and follow-up articles on programming?

Mark Sebald
8722 W Bluemound Rd
Wauwatosa WI 53226

We're working on it. Already in house, expected out in mid 1977, is a very detailed construction project on a 6502 computer system; and we're working on getting articles for several other varieties. "Easily available" is taken to mean that most parts are found in the catalog sheets of hobby distributors.

PRAISE FROM "DOWN UNDER"

Please find enclosed order for US ($30), being 3 years subscription renewal to BYTE (as from January 77). May the high standard of articles continue!

G N Gould
Sydney Hospital
Biochemistry Dept
Macquarie St
Sydney 2000 AUSTRALIA

COMPUTER LANGUAGE PTERODACTYLS, AND OTHER BEASTIES

I write primarily in response to Mr Skye's letter in your August issue. I can only conclude that he had been with IBM too long, otherwise he would not attempt to debase the 8080 with FORTRAN or PL-I. FORTRAN is a virtual pterodactyl, flying on solely by inertia, whereas PL-I is much better, but too rambling in construction. If he indeed takes up the admirable task of writing a high level compiler for the 8080, he would be better advised to base his compiler on a fully structured language such as PASCAL.

Inasmuch as PASCAL was originally devised as a pedagogical tool intended for use in examples of systems programming, it does not have a defined IO structure. In this aspect Mr Skye would be quite justified in reverting to PL-I. PASCAL also lends itself readily to modifications which would allow compile time extensibility in several areas. This is definitely to be preferred over add on "features" which take exception to structure, syntax, grammar, or common sense in any language.

Whatever the final characteristics of Mr Skye's language, it may well become the hobbyist's first or second programming language, due to early availability. Just as with natural languages, the language in which one program affects his approach to programming as a whole, and the first or primary language used tends to influence all later programming.

It is therefore the duty of the language designer to attempt to instill the rudiments of proper programming practices and style in the novice by designing languages which encourage or require such practices. It is, admittedly, not easy to forego the use of some thrilling bit of "trick" code merely because it is configuration dependent, poorly documented, grossly unstructured, or difficult to follow when encountered unexpectedly in the code; however, it will be appreciated later, and practice helps firm the will. The best solution, by far, is to reduce the availability of such tricks until the user has outgrown his programming adolescence.

Small tricks may be introduced in the code *produced* by the compiler if they are suitably documented. In fact, the reduced resources of the average microcomputer installation provides fertile ground for a well written optimizing compiler. If optimization of tricky output is included in a compiler, it is suggested that a section of the user's manual be devoted to the discussion of each instance, giving examples and a full explanation of how it works and why it was done in that manner. It is also to be suggested that optimization be a user option if included, as it is usually much easier to debug unoptimized code, than optimized code when finished.

I will gladly enter into correspondence with anyone who wishes to discuss or debate the features which should properly be included in a programming language, and why (or why not).

P M Lashley
Director of Computing CSCS
POB 764
114 S Bullard St
Silver City NM 88061

Program structure should be looked upon as the language level equivalent of an integrated circuit used by the hardware designer. Why reinvent the DO or IF statements when you can get a language structure prepackaged to do the work? Why reinvent the NAND gate when it can be bought four per package in a 7400? And debugging with standard packages is so much easier, since function is checked rather than internal details. Tiny BASIC and its later full function relatives are just a start in the right direction.

APL CHARACTER ROMS?

When APL becomes available for 6800s and 8080s, it will be nice to have the APL character set, too. In view of the profusion of television displays based on the Motorola MCM6570 series character generator chips, I investigated the practicality of obtaining an MCM6570 series generator for APL. My initial enthusiasm was almost quenched by my local Motorola representative, who informed me that although the unit price of a custom 6570 would be only $8.50, the minimum order would be 500 units and the custom-masking charge, a cool $1000.

While I can't justify spending $5250 ($8.50 X 500 + $1000) for one or two chips, I wonder how many people would be willing to spend $10.50 (5250 ÷ 500)? Or would one of the television typewriter manufacturers be willing to take the plunge, design and market an APL television typewriter, and concurrently finance and vend the APL 6570?

These approaches to the design of the new chip should be considered:

1. By omitting approximately four "noncritical" APL characters — ie: characters not used to represent APL functions — the entire character set, including overstruck characters, can be generated by one chip. This would automatically make any 6570 based television typewriter an APL television typewriter by simple chip swapping.
2. Devoting a full chip to those APL characters that have no ASCII counterparts, the full APL character set and full ASCII character set, including all legal (and some illegal) APL overstrikes, can be accommodated using a standard ASCII 6570 as well. Required modifications to the television typewriter with this approach would include a chip select bit for each character in the refresh buffer, addition of chip selection circuitry in the video generator, and redesign of any cursor circuitry (like that of the Processor Technology VDM-1) that depends on using only 7 bit ASCII.

Roderick Montgomery
52 Birch Av
Princeton NJ 08540

Creating a demand is what is needed. Would an APL enthusiast be willing to pay $52.50 for an APL character generator? If that were the case, all it would take would be 100 such people to get together, buy 500 ROMs and use only 100. (Or better, give each purchaser 5 ROMs to do with as he or she pleased.) However, demonstrating a market interest in the products is a better way. Let's see how many BYTE readers are really into APL, document that, and use it as a message to potential manufacturers.

BELL 103 MODEMS NEEDED

It seems to me that as the hobbyist and small business computer field continues to develop, data communications will become increasingly useful and popular. Because the Bell 103 type data communications hardware interface is already a broadly accepted interface, I intend to use it and hope it will be widely used by other hobbyists and small business operators (at 30 and 10 characters per second).

I have a Tarbell cassette interface, and I intend to use it extensively in my system. However, the fact that no tape interface seems to be evolving as a hardware standard is creating a problem in the exchange of tapes by microcomputer users.

Is it not easily possible to use an originate answer modem as a tape interface? Wouldn't this be an ideal hardware standard for the exchange of cassette tapes in our field? I don't have the time now to describe all of the potential cost and flexibility advantages of such an idea, but I'm sure they can be easily imagined.

Stephen T Moore
Moore Research
POB 1562
Sacramento CA 95814

I think modem recording on tape has been tried . . . with less than optimal results due to the old "wow and flutter" problem. Besides, there are manufacturers now claiming that by using special techniques they can get 400 bytes per second versus communications rates; so why be stuck with a low rate?

STANDARDS

I am very confused about the plethora of cassette data recording "standards" presently available to the computer hobbyist. The more I read about them, the more confused I get, and I am pretty sure that I cannot be the only hobbyist out here with this difficulty. If you could answer the questions below for me, I think you will be performing a noteworthy service for many of your readers:

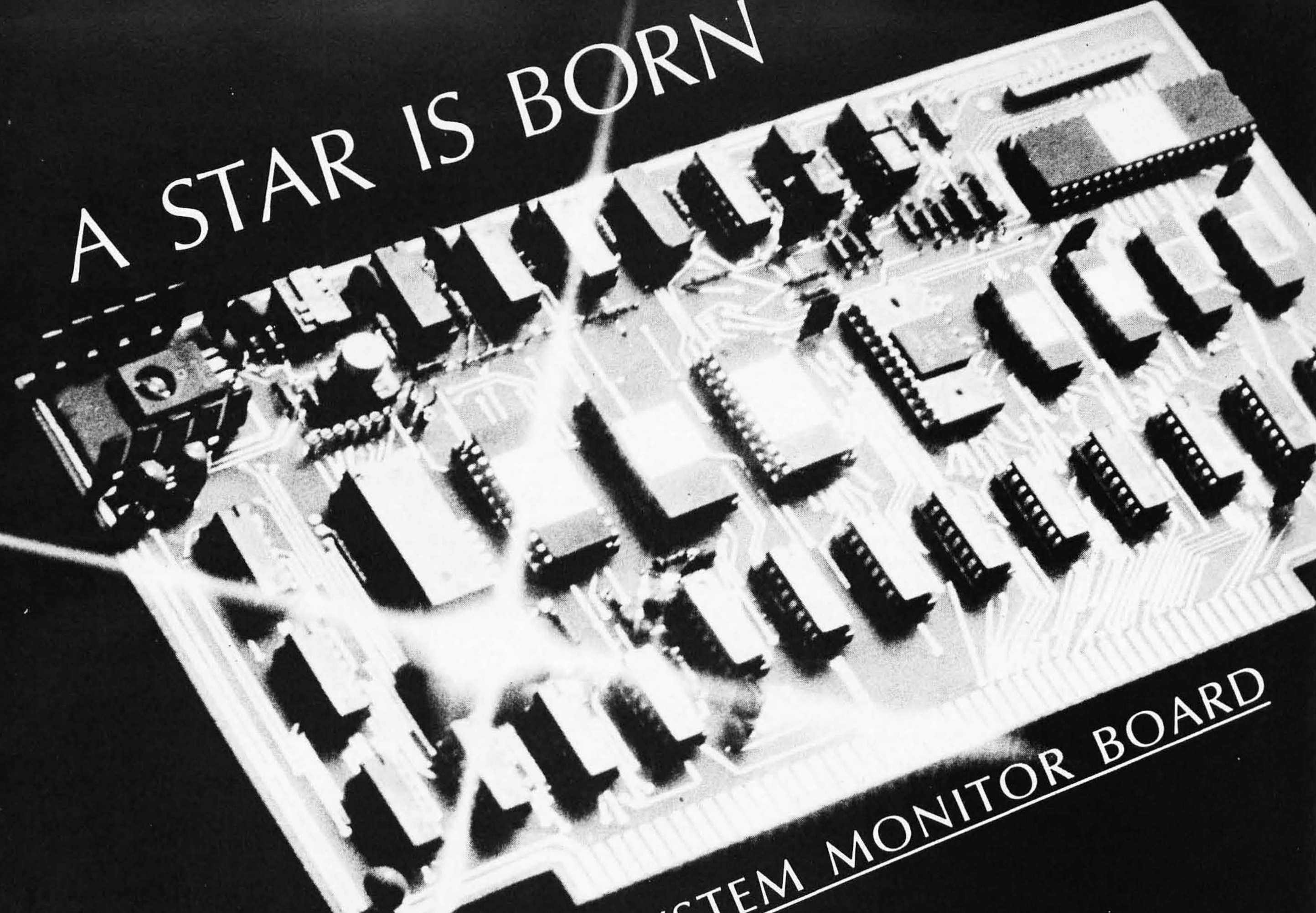
1. Which "standards" are presently in use?
2. Which are gaining/losing favor with hobbyists?
3. Which are compatible with MITS Cassette BASIC?
4. Which are easiest to implement in hardware/software?
5. Which system is the fastest?
6. Is there any relationship between these "standards" and the National Multiplex system advertised in BYTE?
7. Is there a consensus at BYTE about what system you would prefer to load MITS BASIC and to store programs on an Altair 8800?

I realize that the answers to these questions could be both involved and lengthy, but any help you could give me would be greatly appreciated.

Chessman Kittredge III
14 El Sereno Ct
San Francisco CA 94127

1. Audio tape recording media vary from manufacturer to manufacturer. MITS uses the ACR board of their own design, with modem

A STAR IS BORN



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like choices of frequencies. Digital Group uses a similar method, but with different frequencies. The so called "Kansas City" standard is represented by several different manufacturers, including Southwest Technical Products' AC-30 and PerCom. Motorola is also reported to be using it with its latest evaluation board kit. The Tarbell high speed standard is one of the best in terms of speed of operation, as is a "Kansas City" standard interface operating without redundancy using a 2400 baud data rate.

2. *For audio cassettes, as in all IO operations, unless some other circumstance gets in the way, the faster the operation, the better off you are.*
3. *All IO methods are in principle compatible with MITS Cassette BASIC. The only problem is you probably will need to do a "hack" on that BASIC's object text in order to make it work in nonstandard ways. We have not done that (yet) so the problems to be encountered can only be conjectured . . . but it has been done by more than one user.*
4. *In principal, nearly all of the different audio recording standards can be best implemented with one set of hardware and several software designs for the encoding and decoding algorithms. The hardware minimum is an output (optionally filtered) from a TTL gate or equivalent, and an input signal conditioning port (single bit) which converts sine waves (more or less) from the tape into a clean clipped square wave while preserving transition times. Then the different interfaces are typically achieved by simply using a different IO driver program.*
5. *To find out which system is the fastest, look at their data rates. A 300 baud system such as the unmodified "Kansas City" standard is obviously much slower than the same hardware driven at 2400 baud. Also, look at the software being used for formatting the software. A cassette with a raw bit rate of 2400 baud will have an effective bit rate ever so slightly lower if the asynchronous data format of a UART is used, considerably lower if redundant coding is used to check or correct errors, and possibly as low as 30% of the maximum rate if the software employed sends hexadecimal data as ASCII codes for hexadecimal digits.*
6. *The National Multiplex system differs from the normal audio interface only in the greater effective speed possible, and the fact that it ignores the original head drive electronics of an audio channel and achieves greater speed in the electronics by driving the head digitally and directly.*
7. *In a way, yes . . . the faster the better.*

This is by no means an attempt to be complete about the answer. A fuller answer might make good material for an author to supply a detailed comparison aimed at the neophytes just coming aboard.

OPPORTUNITIES

Display Text, Washington DC, has just introduced a Word Processing (text editor) microcomputer for $13,990. The system incorporates 24 K bytes of RAM, a Zilog Z80 chip, two Sycor flippie diskettes, a Thompson 66 line CRT, and a 55 characters per second Qume (typewriter quality) printer.

At that price I expect the system to sell quite well. The marketing outlets are to be selected from independent dealers in most metropolitan areas. (Entrepreneurs take note.)

So what? The opportunities for knowledgeable "microexperts" are unlimited with this system and many others. The significance of the Display Text system versus other systems is its Z80 full page 66 line CRT. System operators can scan a page on the CRT and know exactly how it will look printed. Of course, software by the mega bytes is needed to allow lawyers, insurance agents, doctors, etc, to do things other than word processing on their Z80s.

Never before have we had computers in the home to produce and debug commercially valuable software. I am personally involved with various smaller law offices in an attempt to help them select equipment and software to handle their typewriting, timekeeping, accounting, and case deadlines. This system and other microcomputers for the commercial market could be a very rewarding vehicle for computer enthusiasts who can produce software or hardware assistance.

Allen Swann
Legal Office System Consultant
2510 Oak Trail S 104
Clearwater FL 33516

WUMPUS SOFTWARE?

I have written a machine language version of WUMPUS by Greg Yob. It's a great game. The 8080 program is under 3 K and is completely self-contained: It requires no user PROM subroutines. Anyway, if anyone wants a listing, just send name, address, and $5 to:

Ron Santore
1957 Huasna Dr
San Luis Obispo CA 93401

BROADCAST STATION HANDLER?

Mr Hosking's article "A Ham's Applications Dream" [page 26, October 1976 BYTE] is very dear to my ulterior motives for studying the current revolutionary world of microcomputers.

In addition to being an old "ham" I am currently chief engineer for a small but automated FM broadcast station located at an altitude of 8500 feet (2600 m) in the Sierra Nevadas.

The "automation" system is a solid state device that was built about 20 years ago and is quite reliable but is slowly becoming obsolete. Some foresighted individuals in the broadcast industry have begun to use computer techniques but on a limited and very costly basis.

I have talked to a few microcomputer sales people regarding my application but receive an "I dunno."

Would it be possible for an Altair 8800A or equivalent to, say, sequentially handle 2000 events (switch tape deck, etc) in "real time" and give a "hard copy" (log) for a broadcast station and still be simple enough for an announcer or secretary to program the day's events? (And of course, not cost an arm and a leg?)

Thanks to you and your staff for an understandable approach to a very complicated and otherwise distant world of small systems.

Joe Alvin CE
KMMT
Mammoth Mountain FM Associates Inc
POB 1284
Mammoth Lakes CA 93546

If I were building such an application, I would want at a minimum a floppy disk system, and a good reliable printer. Using a single drive floppy system with 16 K bytes of memory and building custom drivers for all the events, as well as a custom real time clock, such an application could probably be assembled in the $4000-6000 range for parts and subsystems, excluding labor. Would any readers with station automation experience care to share experiences?... CH

PROGRAM "BANK" NEEDED

After a year's exposure to your very fine computer hobbyists' magazine, I feel considerably enlightened on the subject. The articles and advertisements have convinced me of the significance the machines will play in the computer revolution.

Although I confess to be a confirmed computer hobbyist, I do not plan to submit to some of the rigorous repetitive activities that have been proven by other hobbyists. Namely, rewriting proven programs and manually loading the software into my computer.

In many of your articles over the past months, considerable information has been provided on peripherals that interface and load typical programs into a computer's memory. However, I find myself in somewhat of a void regarding how to rapidly load a program into a paper or cassette tape reader.

Is there a company or group that will translate software into a paper or cassette tape for a nominal fee? Is there a program "bank" where the hobbyist can order proven software already on paper or cassette tape? Is there available to the hobbyist a translator that can perform the same?

Any articles or services that might illuminate these questions will be of great help to me and I'm sure to other computer hobbyists.

Laurence P Williams W5IIQ
111 Bradford Cir
Ocean Springs MS 39564

See the information currently in BYTE regarding optical scanning of printed bar codes, and watch BYTE for information regarding clubs and other sources of software. We expect to be providing a software library of machine readable PAPERBYTES™ and SHEET PROGRAMS™ using the printed bar code techniques. Watch future issues of BYTE for information on the PAPERBYTES™ project. (PAPERBYTES™ and SHEET PROGRAMS™ are trademarks of BYTE Publications Inc.)

MORSE REACTIONS TO OCTOBER

I do believe filling your October cover with "BYTE" in Morse code was a *bit* self-centered. (–... –.–– – .) Although the picture of Joseph Henry's telegraphy key was very interesting.

To remark on Hickey's article, "The Computer .... Versus .... Hand Sent Morse Code," I must say that it was very good. But an interesting point came up when I read it. If every amateur radio station used computers in sending and receiving Morse code there would be no need for Morse code. Each station could, and might as well, just use ASCII. Of course the use of ASCII would eliminate the use of telephone lines for teletype. This would not be good for phone companies but businesses and people renting time on a larger system could benefit from the use of the air transmissions. I hope this idea could be developed further.

Mark Lentczner
445 Third St
Brooklyn NY

There is only one problem, though. Amateur radio is amateur; commercial messages are not allowed on the air to amateurs. However, an amateur radio communications net for passing games, personal use programs, etc, back and forth would be quite legitimate within the constraints of being amateur. We're looking for articles to explore that possibility using established computer network software concepts presently used only by the "biggies."

As for the cover issue, isn't the cover of a magazine supposed to advertise its name???

AGGRESSION BY COMPUTER

Our faculty, staff and students are delighted with the way BYTE has developed. We look forward each month to receiving the next issue.

Every day we hear "the computer is responsible!" Business and government are experiencing problems in computer data processing. Many of the difficulties are in relationships with the consumer public. Recipients are invariably frustrated in coping. I am researching "case studies" involving people who are having troubles created by the alleged computer error. I would like to hear from these people describing their situations and what steps they went through in solving, or attempting to solve the difficulties. All responses will be treated confidentially.

Dr Richard A Bassler
Associate Professor of Computer Systems Applications
CTA-B The American University
Washington DC 20016

HANGMAN?

I have bought several issues of your magazine and have enjoyed reading them very much. Although I am new to programming, and do not have a microsystem, I have access to an IBM 370/158 and an IBM 1130 computer. I am learning much from BYTE on programming.

Please, if you know of one, give me the name of a book or an article on games for computers, namely HANGMAN. The language can be in assembler, Fortran, Basic, or PL/1. I would appreciate this very much, as I have hacked my brains out trying to figure that one out.

Robert Todd
1815 N Boomer Rd Apt F-20
Stillwater OK 74074

See page 118 of 101 BASIC Games, *a 250 page paperbound book available for $7.50 plus $.50 postage/handling from Software Distribution Center, Digital Equipment Corp, Maynard MA 01754. This book contains a complete listing of the program, written by Kenneth Aupperle of Melville NY. See also, page 18 of* What To Do After You Hit Return, *published for $6.95 by PCC, POB 310, Menlo Park CA 94025, for a description of how to use such a game. (To get the game program itself, order HANGMN for $3 in paper tape form.)*

DATA BASE MANAGEMENT INFORMATION ?

I am a charter subscriber to BYTE magazine, and very much interested in getting into the home computer field. However, I cannot justify it on the basis of it being the "ultimate toy."

I, and possibly many others, could justify it if the home computer could be applied to do useful work around the house.

One application which comes to mind is that of home or small business record keeping. This brings up the complex subject of data base management systems.

I would very much appreciate a dissertation in BYTE on the design and implementation of data base management. It could be presented as if the user had an Altair 8800 printer, keyboard, and one or more tape cassettes. For example, flowcharts and samples of 8080 code could be used to illustrate how an editor updates a variable length record on cassette by inserting, deleting, or changing data somewhere in the middle of a cassette record.

I believe amateur radio grew as it did because of the social benefits of its applications. Amateur computing must also have a beneficial goal in order for it to grow.

H C Bickel
587 Kiersted Av
Kingston NY 12401 ■

The Impossible Dream Cassette Interface

Daniel Lomax
Community Data Systems
114 E Mohave Rd
Tucson AZ 85705

In May 1975, I had a new Altair 8800, from the original *Popular Electronics* offer, with 256 bytes of memory and no more money. What could I do besides blink lights? The first thing I noticed was that there is an addressable latch in the system, the Interrupt Enabled latch on the 8080, which is nicely buffered and displayed on the Altair front panel. After turning it on and off for a few hours, it occurred to me that, with an earphone, the light might make music, and, after several day's mad programming, some incredibly accurate baroque music emerged, including one recorder piece of which a musician friend – who loaded the data for it – said he had never before been able to hear, being too busy playing it.

After making recordings of the music, the question arose: "If I can record music, why not digital data?" I hadn't heard of the various systems being developed at that time, and my tape recorder is a Ward's Airline $30 cheapie. But, anyway, I recorded various tones on cheap tape, played them back, and looked at them on an oscilloscope. I found that a 2000 Hz tone, linked to the tape recorder through a 0.1 uF capacitor, was reliably reproduced – more or less – with the tape recorder volume turned all the way up, as an 8 V peak to peak "square" wave: That is, "reliably" in the sense that the signal never failed to clip, had no visible glitches, and I could see no missed cycles. There was jitter in the frequency, a few percent.

So, I built a breadboard single channel input interface to look at the signal, capacitor-coupled, and diode-limited between ground and +5, with Altair IN instructions. Though this interface was all TTL – no active linear components – it was still unnecessarily complex, as I will show. Anyway, using one cycle of 1100 Hz as 0 and two cycles of 2200 Hz as 1, I found that I could record data and recover it reliably, using the Altair to time the interval between transitions of the playback signal. According to what I have read, this is impossible. 3M Corp is supposed to have spent many millions of dollars working on cassette data recording systems, only to find that audio cassettes were too unreliable. Therefore, established engineers need read no further (except as entertainment), since this might

About the Author:

Daniel Lomax learned electronics in the physics laboratory at Cal Tech in the mid 60s, but never graduated. Recent work in printing and publishing brought him in contact with a burned out Honeywell Controller which was part of a nonworking Photon phototypesetter, repair of which created a business for him (phototypesetter repair) and taught him TTL logic. He is active in the L-5 Society, a group working to encourage the establishment of permanent human colonies at the L-5 Lagrangian point of the Earth-Moon system. Demonstration of his typesetting proficiencies came to us in the form of excellent typeset manuscripts (which we reset for editorial and stylistic reasons).

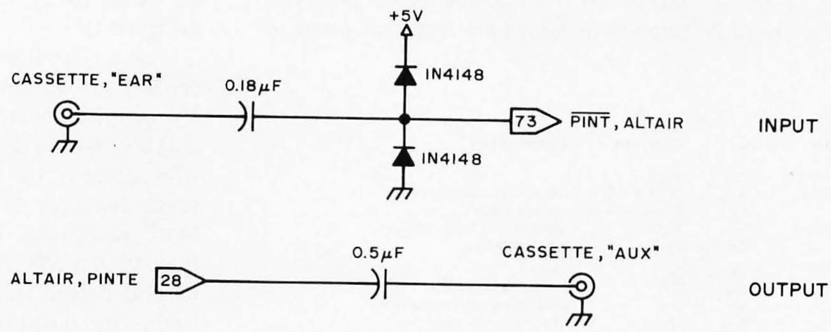


Figure 1: Schematic of the "Impossible Dream" Signal Conditioning Logic. The output consists of simply driving the cassette recorder's input with a TTL level signal. The 0.5 uF capacitor is optional, according to the author, and can be replaced by a direct coupling. The input is a simple network to clip the signal coming back from the tape recorder.

be in the same class as perpetual motion and angle trisection with compass and straightedge.

But, if you are an impoverished hobbyist, and would like to store programs and data at more than 1500 baud without spending any money – assuming you have a tape recorder, some capacitors, diodes, and connectors – let us dream the impossible dream together. *[The "unreliability" of a device is not necessarily dependent upon the modulation method alone. This method hardly contradicts any principles of information theory . . . .* CH*]*

After doing the above experiments, the corporation which owned the Altair folded, and with it my source of income and support for my family. I ended up with the Altair, but had no time to play with it until recently. Meanwhile, I have been following the literature, and have observed all kinds of proposed systems, none of them fast enough for the kinds of applications I have been considering and cheap enough for me to afford. Like Dr Suding *[see "Why Wait?" page 46, BYTE, July 1976]*, I cringe at the thought of waiting 15 minutes to find out that noise has destroyed data and I have to start over.

My original bootstrap loader program was 64 bytes long and included a routine which automatically set the appropriate timing value by examining a string of zeros which preceded the data on the tape, and which updated that value using the stop bit between each byte. This article, however, describes a shorter loader, not automatically self-adjusting, and the hardware has been practically eliminated.

It seems I had overlooked the fact that in the Altair there is, in addition to the sense switches, one free input channel – of sorts – PINT. If PINT cannot be used for some reason, a program can be written using normal input channels. Also, there is no reason to output two cycles for a single bit,

Listing 1: Minimum Hardware Cassette Output Program. This program is a stand alone method of recording data starting at location BUFFER on to the recorder through the Altair PINTE line. This program terminates when the page address is zero. A more general program could of course be written by changing the initial conditions, and the end of execution test at locations 046 and 047. Note that in the listings of this article, the notation <0> is used to indicate page addresses. The programs shown can be loaded at any arbitrary page boundary by substituting an octal number (such as 003) for <0> every time it appears.

Split Octal Address	Octal Code	Label	Op	Operands	Commentary
	377	SSW	EQU	377	
	200	BUFFER	EQU	200	
<0>/000	041 200 <0>	• START	LXI	H,BUFFER	set initial output pointer;
<0>/003	061 200 <0>		LXI	SP,BUFFER	set the stack;
<0>/006	333 377	LOAD	IN	SSW	input timing value;
<0>/010	117		MOV	C,A	save it in C;
<0>/011	027		RAL		set carry if SSW7 active;
<0>/012	324 055 <0>		CNC	ZERO	if not, output data '0';
<0>/015	322 006 <0>		JNC	LOAD	and if not, look again;
<0>/020	017		RRC		recover timing value bit 7;
<0>/021	117		MOV	C,A	save it in C;
<0>/022	315 066 <0>	NEXT	CALL	ONE	output '1' as start bit;
<0>/025	176		MOV	A,M	look up data byte;
<0>/026	006 010		MVI	B,010	load bit counter to one byte length;
<0>/030	007	BIT	RLC		set carry if data '1';
<0>/031	334 066 <0>		CC	ONE	if '1', output '1';
<0>/034	324 055 <0>		CNC	ZERO	if not '1'; output '0';
<0>/037	005		DCR	B	decrement bit counter;
<0>/040	302 030 <0>		JNZ	BIT	if byte incomplete, output next bit;
<0>/043	315 055 <0>		CALL	ZERO	byte complete, output stop bit;
<0>/046	054		INR	L	advance output pointer;
<0>/047	302 022 <0>		JNZ	NEXT	go output next byte;
<0>/052	166		HLT		page done, halt;
<0>/053	000		NOP		space for
<0>/054	000		NOP		exit jump;
<0>/055	363	ZERO	DI		turn off PINTE;
<0>/056	315 105 <0>		CALL	TIMEA	wait 2C cycles;
<0>/061	373		EI		turn on PINTE;
<0>/062	315 105 <0>		CALL	TIMEA	wait 2C cycles;
<0>/065	311		RET		
<0>/066	363	ONE	DI		turn off PINTE;
<0>/067	315 112 <0>		CALL	TIMEB	wait C cycles;
<0>/072	315 105 <0>		CALL	TIMEA	wait 2C cycles;
<0>/075	373		EI		turn on PINTE;
<0>/076	315 112 <0>		CALL	TIMEB	wait C cycles;
<0>/101	315 105 <0>		CALL	TIMEA	wait 2C cycles;
<0>/104	311		RET		
<0>/105	121	TIMEA	MOV	D,C	load timing counter;
<0>/106	025	WAITA	DCR	D	count cycles;
<0>/107	302 106 <0>		JNZ	WAITA	count until zero;
<0>/112	121	TIMEB	MOV	D,C	load timing counter;
<0>/113	025	WAITB	DCR	D	count cycles;
<0>/114	302 113 <0>		JNZ	WAITB	count until zero;
<0>/117	311		RET		

Listing 2: Minimum Hardware Cassette Bootstrap Loader. This program is used to read the data recorded on a tape by the output program of listing 1. The program is set up to assume coordination through the Altair interrupt line $\overline{PINT}$, but the method could be applied using timing loops on input as well.

Split Octal Address	Octal Code	Label	Op	Operands	Commentary
	200	BUFFER	EQU	200	
<0>/000	041 200 <0> *	START	LXI	H,BUFFER	set initial load pointer;
<0>/003	061 200 <0>		LXI	SP,BUFFER	set the stack;
<0>/006	066 000	CLEAR	MVI	M,000	clear initial load location;
<0>/010	303 106 <0>		JMP	SET	go to work;
<0>/070	063	INT	INX	SP	reset
<0>/071	063		INX	SP	stack pointer;
<0>/072	270		CMP	B	was interrupt immediate?
<0>/073	312 110 <0>		JZ	INTE	if so, try, try again;
<0>/076	326 001		SUI	001	set carry if data '1';
<0>/100	176		MOV	A,M	look up byte under construction;
<0>/101	027		RAL		rotate through carry;
<0>/102	167		MOV	M,A	put it away;
<0>/103	332 122 <0>		JC	BYTE	if byte complete, go advance pointer;
<0>/106	333 377	SET	IN	SSW	input timing criterion (sense switches);
<0>/110	107		MOV	B,A	hold for comparison;
<0>/111	373	INTE	EI		enable interrupt;
<0>/112	000		NOP		give it time to act before timing;
<0>/113	075	COUNT	DCR	A	time period until interrupt;
<0>/114	302 113 <0>		JNZ	COUNT	A>0 at interrupt, data '0';
<0>/117	303 117 <0>	LOOP	JMP	LOOP	A=0 at interrupt, data '1';
<0>/122	054	BYTE	INR	L	advance load pointer;
<0>/123	302 006 <0>		JNZ	CLEAR	if not end of page, go load next byte;
<0>/126	052 001 <0>		LHLD	START	restore initial load pointer;
<0>/131	351		PCHL		transfer control to object program;

Listing 3: Timing Test Patches to Listing 2. These patches are used to verify the timing for the outputs by testing the actual timing values received for each bit, storing them instead of the data.

Split Octal Address	Octal Code	Name	Op	Operands
			ORG	113
<0>/113	074	COUNT	INR	A
			ORG	076
<0>/076	000		NOP	
<0>/077	000		NOP	
<0>/100	000		NOP	
<0>/101	000		NOP	
<0>/102	167		MOV	M,A
<0>/103	303 122 <0>		JMP	BYTE
			ORG	131
<0>/131	166		HLT	

Listing 4: Dropout Test Patches to Listing 2: These patches are used to look for spurious binary 1 data in a tape filled with binary 0 data. The Altair will halt on any byte which is not 000 (octal).

Split Octal Address	Octal Code	Name	Op	Operands
			ORG	122
<0>/122	054 000	BYTE	CPI	000
<0>/124	312 006 <0>		JZ	CLEAR
<0>/127	166		HLT	

so the revised program looks for one cycle of 2020 Hz as 0, and one cycle of 1470 Hz as 1.

To try the system out, you can use a solderless breadboard, or even just a bunch of jumpers with alligator clips. PINTE (for output to tape) can be picked up on the front panel. Both $\overline{PINT}$ and PINTE can be found on the motherboard, at Altair backplane connector pins 73 and 28, respectively. I have found it convenient, for debugging programs using interrupts, to wire $\overline{PINT}$ to one of the extra switches on the Altair front panel, connecting the center terminal of the switch to ground. For the clipping network, I pick off ground from the motherboard support rails, and +5 V from the front panel. Connect it all up as shown in figure 1.

For a system test, clear the memory, then deposit the output program shown in listing 1 into the memory. Replace the HLT at 000,052 with a JMP START,303. The NOPs will serve as the START address. Set the sense switches to 010, and initiate RUN. Start recording. Wait about five seconds, then switch SSW7 to 1. Let the tape run to its end before stopping the Altair. This test begins by outputting continuous zero bits and then, when SSW7 is turned on, it outputs a start bit in the 1 state, then eight data zeros followed by a stop zero. Then it repeats with another start bit, and so forth.

To read back this data, deposit the bootstrap loader into the memory. Change the PCHL at 000,131 to HLT (166). With the connector out of the earphone jack of the recorder, so you can hear the recording, start playing the tape. When the clean, high pitched tone starts (the train of zeros), stop the tape recorder immediately. Put the connector back in, and turn the recorder volume all the way up. Set the sense switches to 050. Start the recorder, wait a second or so for it to settle, then start the Altair with the RUN switch. The Altair should, when the tape runs into the data and begins transmitting bytes, load for about a half second and then halt. To get out of the halt condition, hold the STOP switch up while you RESET. The memory, from 000,200 to 000,377 should be blank, all zeros. Put 377 into 000,377, and try loading the tape again. 000,377 should come out blank again.

If it doesn't work, tape recorder signal polarity may be reversed between recording and playback. Try reversing the signal and ground leads from the tape recorder to the input network. (Disconnect the output connector and any other common grounds.) If the system then works, interchange the EI and DI instructions in the output program to produce correct results with normal connector polarity.

To verify the timing, you can modify the loader as shown in listing 3. Set the sense switches to 000. Start reading the tape while data is being played back, rather than during the leader zeros as usual. The Altair should quickly halt. At address 000,200, and in sequential addresses, you should find the timing values for each bit as it came in. Make a list of these values, and you should see the data pattern. The value 050 was chosen to be in between the timing values for 0 and 1.

To test tape for dropouts, which will read as spurious 1s, use the bootstrap loader with

the patch shown in listing 4. Start the recorder and Altair as usual for data, with the test tape having been filled with data 000 as in the first test. The Altair will halt if it finds any byte that is not 000. It will also probably halt when the tape ends, from shutoff noise.

The data rate for this system, as described, varies with the data: 1470 baud for all binary 1s, 2020 baud for all 0s. I suspect that it would work with higher data rates; but, for my cheap cassette, the signal level won't drive TTL reliably much above 2 kHz. The addition of an amplifier or zero-crossing detector could compensate for that problem, possibly increasing the data rate by a factor of two to four; of course, a better recorder and better tape would also help.

The key feature of this method of recording data is that the recorded signal is symmetrical: It spends as much time high as low. I found that, if I tried to record unsymmetrical signals on the cassette, the narrower pulses tended to be present only as dips and bulges in the distorted attempt at a sine wave that the recorder produces.

Figure 2 shows the waveforms present in the system under various conditions. If the cassette output does not produce a reliable interrupt, try a larger value capacitor or a lower frequency (increase the sense switch setting from 010).

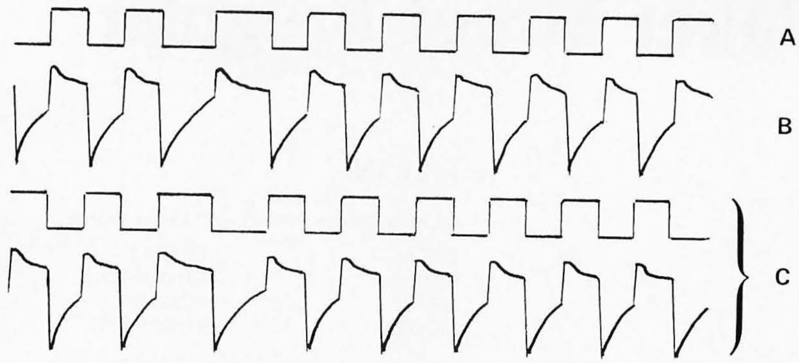


Figure 2: Tracings of Typical Signals.
a. The PINTE output signal from the Altair which is fed to the recorder.
b. The input signal clipped and seen by $\overline{PINT}$ when a recording of (a) is fed back into the computer.
c. Typical signals, in the case where polarity is reversed. See text for a complete explanation.

A final note: Timing values (sense switch settings) described in this article are appropriate for an Altair 8800 with memory wait cycles. If the processor is running at 2 MHz with no wait states, try 014 as sense switch setting for the Output Program, and 074 for the bootstrap loader.■

Baker Street Irregular

Robert Baker
15 Windsor Dr
Atco NJ 08004

FILL IN:

4 Letter Words

BETA
CASE
MEAN
MODE

5 Letter Words

GAMMA
RANGE

6 Letter Words

DECILE
EXCESS
MEDIAN
MOMENT

7 Letter Words

DENSITY
GROUPED
POISSON
THEOREM

11 Letter Words

COEFFICIENT
CONDITIONAL
CORRELATION
EXPECTATION
MULTINOMIAL

8 Letter Words

BINOMIAL
CUMULANT
HARMONIC
KURTOSIS
MARGINAL
QUARTILE
SAMPLING
SKEWNESS
VARIABLE
VARIANCE
WEIGHTED

9 Letter Words

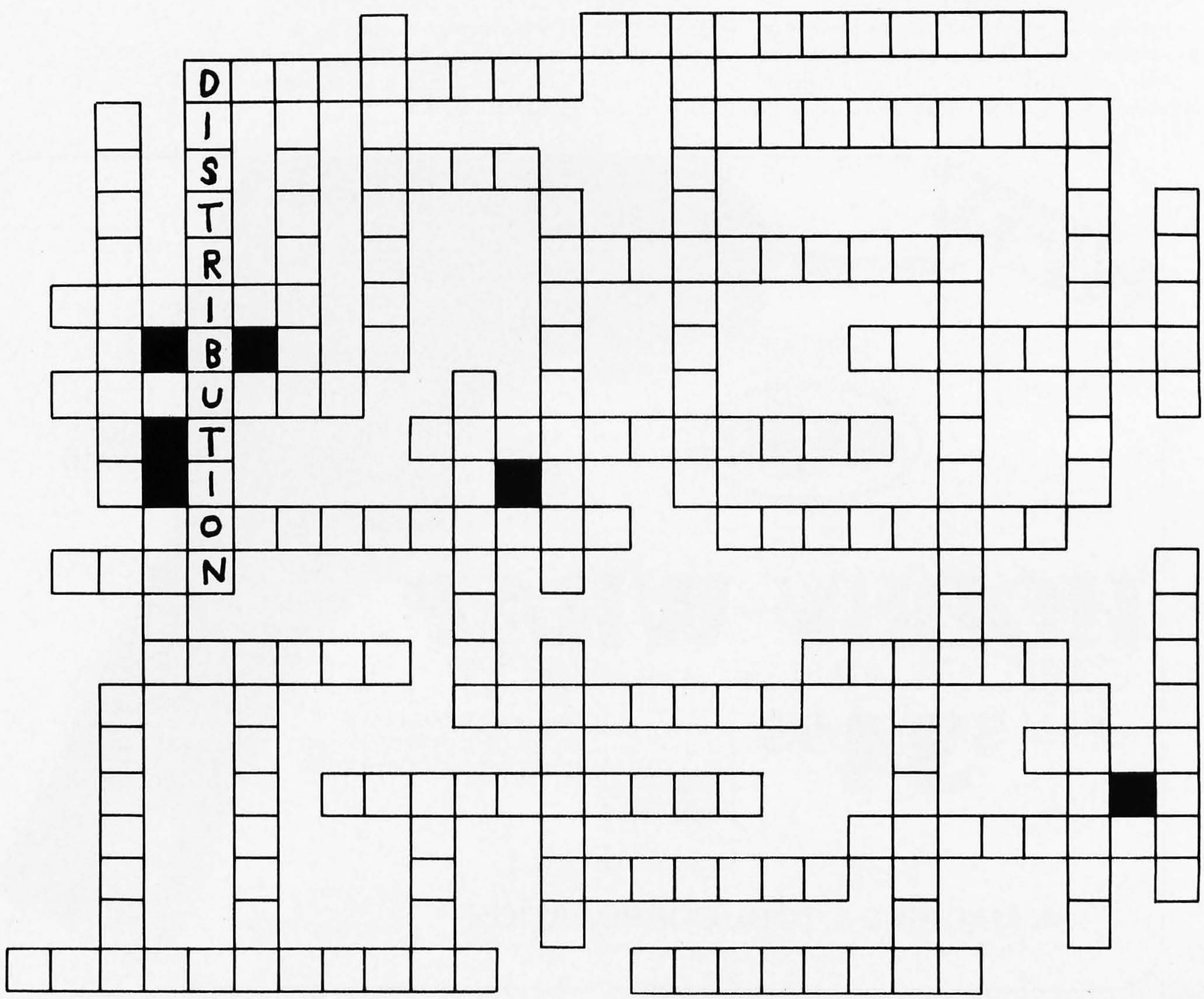
DEVIATION
EMPIRICAL
GEOMETRIC
VARIATION

10 Letter Words

ARITHMETIC
CUMULATIVE
PERCENTILE
REGRESSION

12 Letter Words

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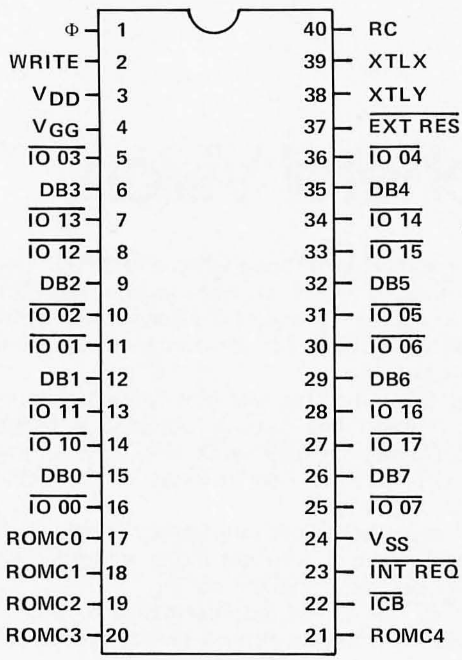
Address____________________________

City/State/Zip________________________

Microprocessor Update:

The F8 System

Robert Baker
15 Windsor Dr
Atco NJ 08004



Pin Name	Description	Type
DB0 – DB7	Data bus lines	Bidirectional
Φ, WRITE	Clock lines	Output
IO 00 – IO 07	IO port zero	Bidirectional
IO 10 – IO 17	IO port one	Bidirectional
RC	RC network pin	Input
ROMC0 – ROMC4	Control lines	Output
EXT RES	External reset	Input
INT REQ	Interrupt request	Input
ICB	Interrupt control bit	Output
XTLX	Crystal clock line	Output
XTLY	External clock line	Input
V_{SS} = 0 V, V_{DD} = +5, V_{GG} = +12 V	Power lines	Input

Figure 1: Pin designations for the 3850 central processing unit chip.

The architecture of the F8 microprocessor is rather unique in design since the various system functions are deliberately divided among the several basic circuits of the F8 family instead of being centralized within a single processor. The currently available F8 system components include the following devices:

3850	central processing unit
3851	program storage unit
3852	dynamic memory interface
3853	static memory interface
3854	direct memory access

These devices are interconnected by an 8 bit time multiplexed data bus for addressing and data functions, along with a 7 bit control bus for system coordination and synchronization. System timing signals are derived from a master clock generator with a maximum frequency of 2 MHz within the 3850 processor. The clock output of the processor divides the machine cycle into a number of discrete phases dependent on the type of instruction being executed. Multiple memory references may require as many as three machine cycles as controlled by the processor's WRITE clock. Besides these two clock lines, the remaining five lines of the control bus are the Read Only Memory Control (ROMC) outputs. They are derived from the processor's internal control read only memory as a function of each instruction and are listed in detail within the Fairchild documentation along with a description of the corresponding operation of each F8 component.

A 16 bit address structure allows addressing of up to 64 K bytes of memory containing any combination of programmable stor-

age units or standard read only memory and programmable memory with the appropriate interface devices. Instead of transmitting an address to all the individual memory devices during each processor cycle, the memory devices maintain their own 16 bit program counter. Every programmable storage unit or memory interface updates its program counter just as a processor would, incrementing the register each time an instruction is fetched or loading a new address when a jump instruction is encountered. For relative addressing, each device also has a built-in hardware adder to compute the displacement from the current program counter value.

A second register, known as the stack register, backs up the program counter in all memory elements during subroutine calls and interrupts. When a subroutine or interrupt handler address is jammed into the program counter, the return address, the old contents of the program counter, is saved in the stack register.

Every memory chip also contains a 16 bit pointer register called the data counter which can be addressed and loaded from the 3850 processor. All memory references during memory reference instructions utilize the data counter which implicitly indicates an object address.

The 3850 Processor

The 3850 processor is the heart of the F8 microprocessor system, containing the data manipulation logic that can perform either binary or decimal arithmetic. A control unit decodes 8 bit instructions controlling execution of logic within the processor and generating control signals for the other chips in the system. The processor chip pin assignments are shown in figure 1. Figure 2 indicates the three different modes of system clock generation: resistor capacitor network, crystal, or external clock; that may be used to provide a typical 2 μs cycle time.

The 3850 processor has a single 8 bit accumulator, and a scratchpad consisting of 64

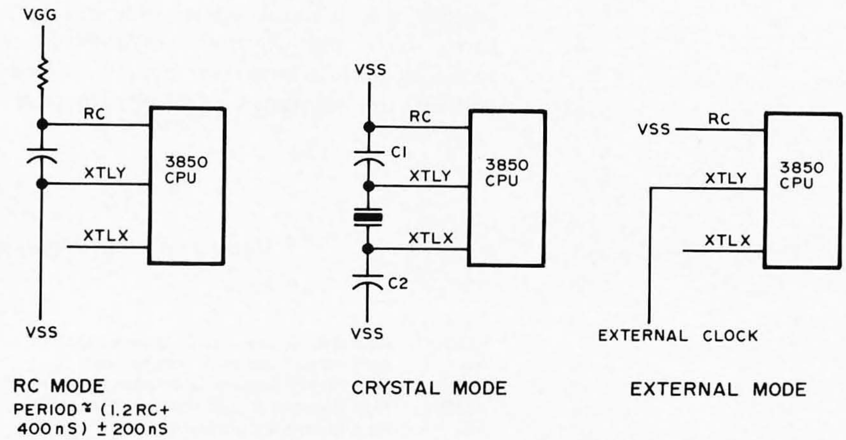


Figure 2: Three modes of clock generation for the F8 system.

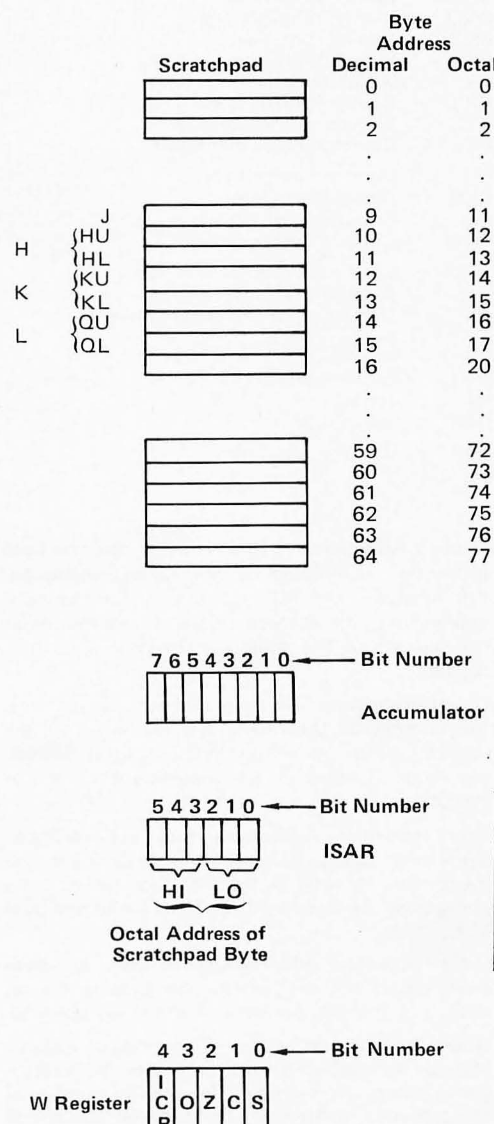


Figure 3: The programmable registers for the 3850 processor.

Information and diagrams courtesy of Fairchild Semiconductor from their F8 Circuit Data Book and F8 Microprocessor Programmer's Guide.

8 bit general purpose registers that are addressed by a 6 bit indirect scratchpad address register as shown in figure 3. The W register, a 5 bit status register, indicates sign, carry, zero, and overflow conditions as a result of various processor operations and contains the interrupt control bit. The processor chip also contains two 8 bit, bidirectional, IO ports with output latches for transferring data to and from the processor.

Any of the over 60 machine instructions together with the eight different addressing modes, shown in table 1, may be used to manipulate or operate on 8 bit data con-

Table 1: F8 instruction set and addressing modes.

ADC	Add data counter with accumulator
AI	Add immediate with accumulator
AM	Add binary accumulator with memory
AMD	Add decimal accumulator with memory
AS	Add binary accumulator with scratchpad register
ASD	Add decimal accumulator with scratchpad register
BC	Branch on carry
BF	Branch on false condition
BM	Branch if negative
BNC	Branch if no carry
BNO	Branch if no overflow
BNZ	Branch if no zero
BP	Branch if positive
BR	Absolute branch
BR7	Branch if ISAR is not 7
BT	Branch on true condition
BZ	Branch on zero condition
CI	Compare immediate
CLR	Clear accumulator
CM	Compare with memory
COM	Complement accumulator
DCI	Load data counter immediate
DI	Disable interrupt
DS	Decrement scratchpad register
EI	Enable interrupt
INC	Increment accumulator
IN	Input
INS	Input short
JMP	Jump
LI	Load accumulator immediate
LIS	Load accumulator short
LISL	Load ISAR – Lower 3 bits
LISU	Load ISAR – Upper 3 bits
LM	Load memory
LNK	Link carry into accumulator
LR	Load register (5 types) Scratchpad Program counter ISAR Status Data counter
NI	Logical AND accumulator immediate
NM	Logical AND memory accumulator
NOP	No operation
NS	Logical AND scratchpad and accumulator
OI	Logical OR immediate
OM	Logical OR memory with accumulator
OUT	Output
OUTS	Output short
PI	Push program counter into stack register Set program counter to new location
PK	Push program counter into stack register Set program counter from scratchpad
POP	Put stack register into program counter
SL	Shift left
SR	Shift right
XDC	Exchange data counters
XI	Exclusive OR immediate
XM	Exclusive OR accumulator with memory
XS	Exclusive OR accumulator with scratchpad

Implied Addressing – The data for this one byte instruction is implied by the actual instruction. For example, the POP instruction automatically implies that the content of the program counter will be set to the value contained in the stack register.

Direct Addressing – In these two byte instructions, the address of the operand is contained in the second byte of the instruction. The direct addressing mode is used in the input output class of instructions.

Short Immediate Addressing – Instructions whose addressing mode is short immediate have the instruction op code as the first four bits and the operand as the last four bits. They are all one byte instructions.

Long Immediate Addressing – In these two byte instructions, the first instruction byte is the op code and the second byte is the 8 bit operand.

Direct Register Addressing – This mode of addressing may be used to directly reference the scratchpad registers. By including the register number in the one byte instruction, 12 of the 64 scratchpad registers may be referenced directly.

Indirect Register Addressing – All 64 scratchpad registers may be indirectly referenced, using the indirect scratchpad register in the processor. This 6 bit register, which acts as a pointer to the scratchpad memory, may either be incremented, decremented, or left unchanged while accessing the scratchpad register.

Indirect Memory Addressing – A 16 bit indirect address register, the data counter, points to either data or constants in bulk memory. A group of one byte instructions is provided to manipulate this area of memory. These instructions imply that the data counter is pointing to the desired memory byte. The data counter is self-incrementing, allowing for an entire data field to be scanned and manipulated without requiring special instructions to increment its content. The memory interface circuit contains two interchangeable data counters.

Relative Addressing – All F8 branch instructions use the relative addressing mode. Whenever a branch is taken, the program counter is updated by an 8 bit relative address contained in the second byte of the instruction. A branch may extend 128 locations forward or 127 locations back.

tained in the accumulator, scratchpad registers, or any memory location. Instructions referencing scratchpad bytes are the fastest executing F8 instructions, but only the first 16 scratchpad bytes can be referenced directly by instructions. The indirect scratchpad address register must be used to reference the last 48 bytes of the scratchpad but may also be used to address the first 16 bytes as well. Scratchpad registers 9 through 15 have special significance for the F8 system as mentioned later.

The 3851 Program Storage Unit

The program storage unit contains 1024 bytes of read only memory, two independently addressable 8 bit IO ports, a programmable timer, external interrupt control circuitry, and three address registers, called PC0, PC1 and DC. Each program storage unit chip is mask programmed during manufacturing to user specifications, including a 6 bit page select, chip enable, option which corresponds to the upper 6 bits of the address space. This customization at manufacturing time makes it unlikely that the 3851 will ever be used by homebrew computer people; however, it may show up in finished product or kit machines as a place to put the system monitor. The memory access logic of each program storage unit is only activated when the upper 6 bits in the program counter match the program storage unit page select code. With up to 64 possible program storage units, every program counter will

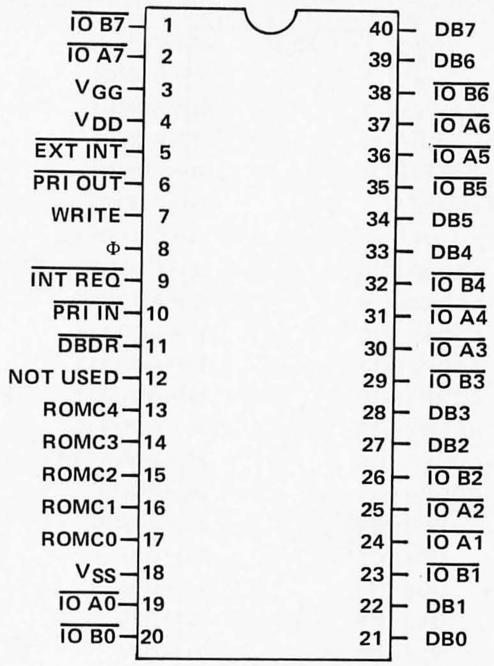


Figure 4: Pin designations for the 3851 program storage unit chip.

Pin Name	Description	Type
IO A0 – IO A7	IO port A	Bidirectional
IO B0 – IO B7	IO port B	Bidirectional
DB0 – DB7	Data bus	Input
ROMC0 – ROMC4	Control lines	Input
Φ, WRITE	Clock lines	Input
EXT INT	External interrupt	Input
PRI IN	Priority in	Input
PRI OUT	Priority out	Output
INT REQ	Interrupt request	Output
DBDR	Data bus drive	Output
V_{SS} = 0 V		
V_{DD} = +5 V	Power supply lines	Input
V_{GG} = +12 V		

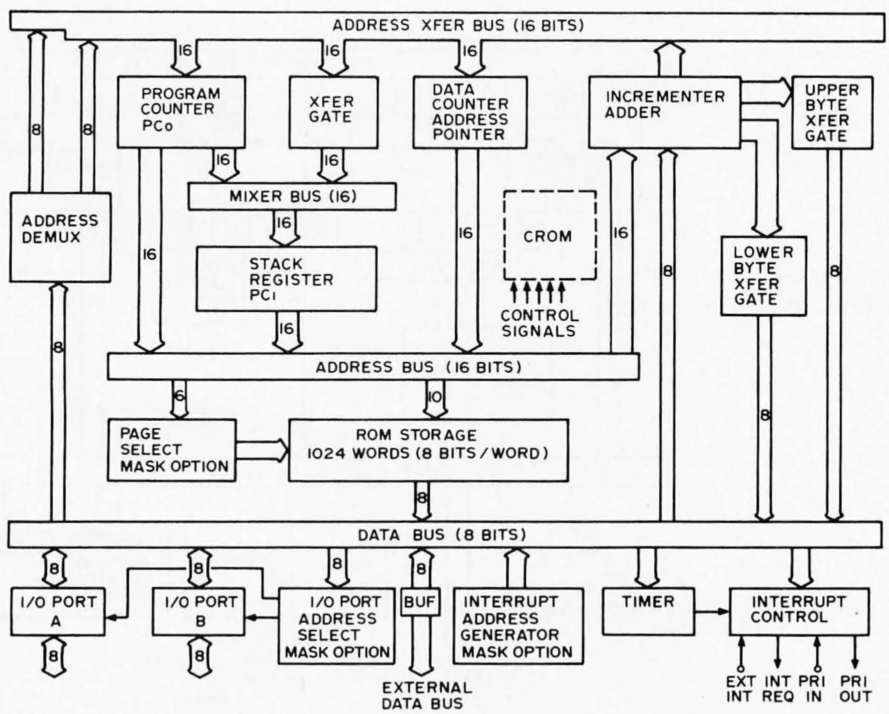


Figure 5: A block diagram of the 3851 program storage unit.

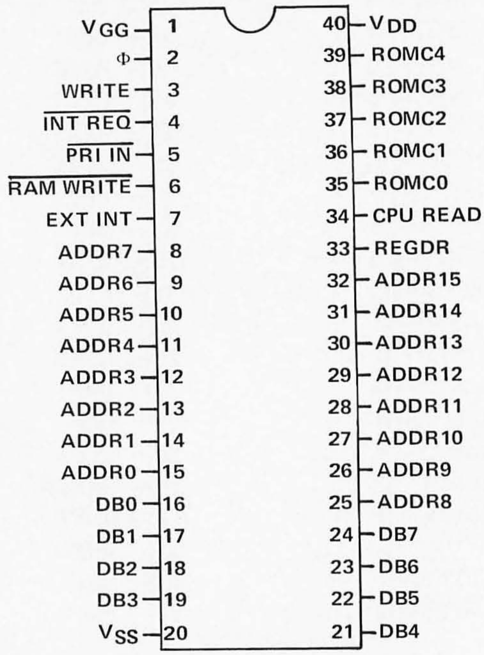


Figure 6: Pin designations for the 3852 dynamic memory interface chip.

Pin Name	Description	Type
DB0 – DB7	Data bus lines	Bidirectional
ADDR0 – ADDR15	Address lines	Output
Φ, WRITE	Clock lines	Input
$\overline{\text{INT REQ}}$	Interrupt request	Output
$\overline{\text{PRI IN}}$	Priority in line	Input
$\overline{\text{RAM WRITE}}$	Write line	Output
$\overline{\text{EXT INT}}$	External interrupt line	Input
REGDR	Register drive line	Input output
CPU READ	CPU read line	Output
ROMC0 – ROMC4	Control lines	Input
V_{SS} = 0 V, V_{DD} = +5 V, V_{GG} = +12 V	Power supply lines	Input

contain the same address but only one chip will detect a page select match and forward an 8 bit instruction to the processor during a fetch cycle in a properly designed system.

The 16 bit program counter provides the memory address of the next instruction to be fetched and transmitted to the processor, while the internal program storage unit logic will increment the program counter after each fetch. The program counter registers of all program storage unit chips are logically connected to the K register of the processor scratchpad, bytes 12 and 13. The contents of all program counter registers may be loaded from the K register or modified by certain instructions. The data counter register, as described earlier, is similarly linked to the H register, bytes 10 and 11, of the processor scratchpad. Each program storage unit contains only one data counter register, so the swap data counters instruction has no effect.

The 16 bit stack register (called PC1) is primarily used as a buffer for the program counter, saving return addresses for subroutines and interrupt handlers. The stack register is logically connected to the K register of the processor scratchpad and may be loaded to or from the K register. Whenever the value of the program counter is saved in the stack register, the value in the stack register is first saved in the K register.

The internal circuitry of the two IO ports within the program storage unit may be selected from one of three manufacturing mask options for different hardware applications: standard pull up, open drain, or driver

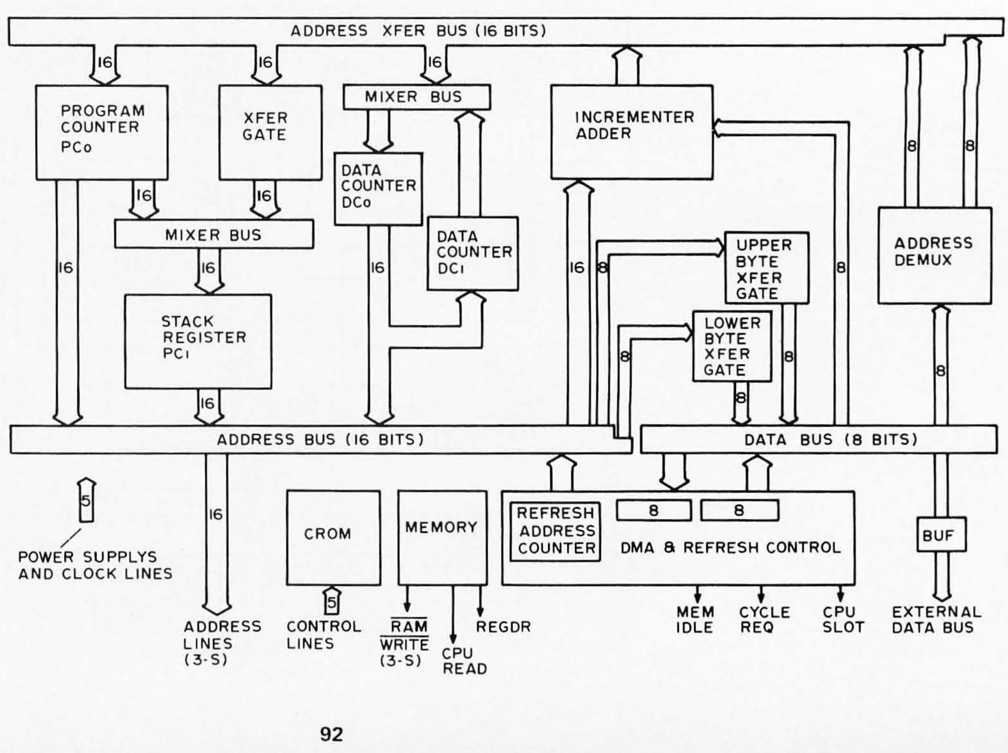


Figure 7: Block diagram of the 3852 dynamic memory interface.

pull up. The programmable timer and interrupt logic are accessed in the same manner as the IO ports with specifically assigned port addresses that are the same in each program storage unit except for the page select bits.

The programmable timer port is a continuously running polynomial shift register that sends a signal to the interrupt control logic every 3.953 ms if the system has a 2 MHz clock. Any numeric value between 0 and 254 loaded to a timer port is decremented once every 31 clock pulses allowing programmed delays of up to 7,905 clock pulses. If 255 is loaded into a timer port, the timer is stopped. When a loaded timer count is decremented to zero, a timer interrupt is generated and will be transmitted to the processor if timer interrupts have been enabled via a control code loaded to the interrupt port.

A mask programmed 16 bit interrupt vector is pushed into the program counter whenever an interrupt from the interrupt control of the program storage unit is serviced. However, bit 7 of the interrupt vector is set by the interrupt control and is not mask programmed.

Pin assignments of the 40 pin program storage unit chip are shown in figure 4 with a block diagram in figure 5. Each chip requires +5 V and +12 V DC power supplies with total power typically less than 275 mW.

The 3852 Dynamic Memory Interface

The dynamic memory interface provides the necessary address and control lines to interface up to 64 K bytes of programmable



Figure 8: Pin designations for the 3853 static memory interface chip.

Pin Name	Description	Type
DB0 – DB7	Data bus lines	Bidirectional
ADDR0 – ADDR15	Address lines	Output
Φ, WRITE	Clock lines	Input
MEMIDLE	DMA timing line	Output
CYCLE REQ	RAM timing line	Output
CPU SLOT	Timing line	Output
CPU READ	RAM timing line	Output
REGDR	Register drive line	Input output
$\overline{\text{RAM WRITE}}$	Write line	Output
ROMC0 – ROMC4	Control lines	Input
V_{SS} = 0 V	Power lines	Input
V_{DD} = +5 V		
V_{GG} = +12 V		

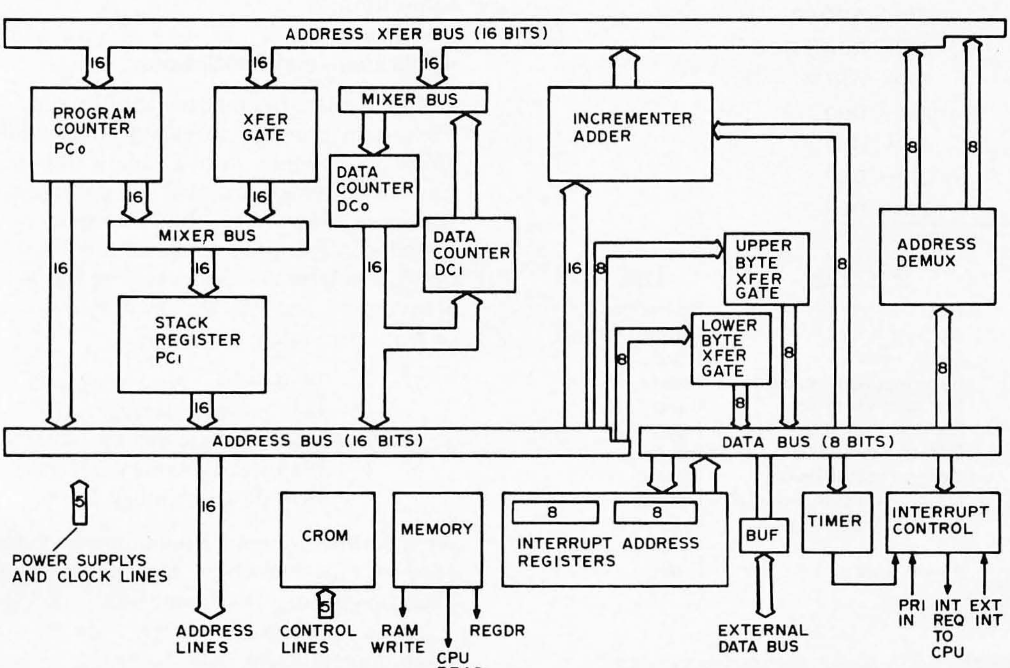
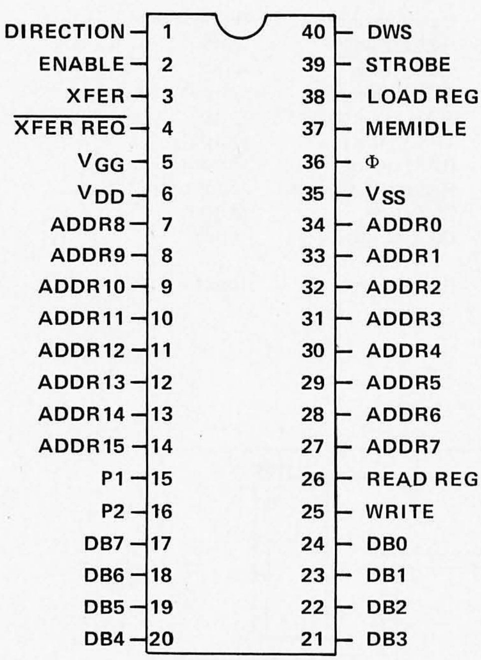


Figure 9: A block diagram of the 3853 static memory interface.

memory, read only memory, or combinations of the two to the F8 processor. It contains the same address registers as the 3851 program storage unit but it has two data counter registers (DC0 and DC1). DC1 is used as a temporary storage buffer for DC0 and the swap data counters instruction may be used to exchange the contents of the two counters. The dynamic memory interface has no chip select mask since the entire program counter address is passed from the dynamic memory interface to the attached memory which in turn must decode the appropriate chip select lines. Two addressable ports provide direct memory access capabilities in conjunction with the 3854 direct memory access chip discussed later and also provide refresh control for external dynamic MOS memory chips. Figure 6 shows the pin assignments of the 40 pin package while figure 7 shows a block diagram of the interface.



Pin Name	Description	Type
DB0 – DB7	Data bus lines	Bidirectional
ADDR0 – ADDR15	Address lines	Output
Φ, WRITE	Clock lines	Input
LOAD REG/READ REG	Registers load/read line	Input
P1, P2	Port address select	Input
MEMIDLE	Memory idle line	Input
XFER REQ	Transfer request line	Input
ENABLE, DIRECTION	Control status lines	Output
DWS, XFER	DMA write slot, transfer	Output
STROBE	Output strobe line	Output
V_{SS} = 0 V, V_{DD} = +5 V, V_{GG} +12 V	Power lines	Input

Figure 10: Pin designations for the 3854 direct memory access chip.

The 3853 Static Memory Interface

The static memory interface chip is very similar to the dynamic memory interface except it is used to interface only static memory to the processor and does not have direct memory access capabilities. In addition, it contains local timer and interrupt control ports like those in the program storage unit together with two additional programmable interrupt vector registers. Figure 8 shows the pin assignments for the 40 pin chip and figure 9 shows a block diagram of the static memory interface.

The 3854 Direct Memory Access

The direct memory access chip, together with the dynamic memory interface chip, allows high speed data transfers between peripherals and memory. All direct memory access data transfers are made during the second and third clock pulses of each instruction cycle without affecting program execution time. Up to four direct memory access chips may be used in a single F8 system and an external device, including another microprocessor, may be connected to the system through these chips.

The direct memory access interface contains three internal registers that are addressed as four separate IO ports: a 16 bit address register holds the address of the next memory byte to be accessed for a transfer; a 12 bit byte count register allows blocks of up to 4 K bytes to be transferred; and a 4 bit control register determines the direct memory access operation to be performed. Figure 10 shows the pin assignments and figure 11 is a block diagram of the direct memory access unit.

Applications and Conclusions

For personal computer applications, the F8 system provides an easy to use building block architecture with a narrow bus structure simplifying hardware design and construction. Figure 12 shows a general F8 system configuration implementing all of the possible system components. The F8 system architecture restricts the maximum number of chips per system as follows:

1 – 3850 central processing unit
64 – 3851 program storage units
1 – 3852 dynamic memory interface
1 – 3853 static memory interface
4 – 3854 direct memory access

At the other extreme, a minimum F8 system requires only two chips, the 3850 processor and a single program storage unit.

Since all program storage units are mask programmed during manufacturing, software

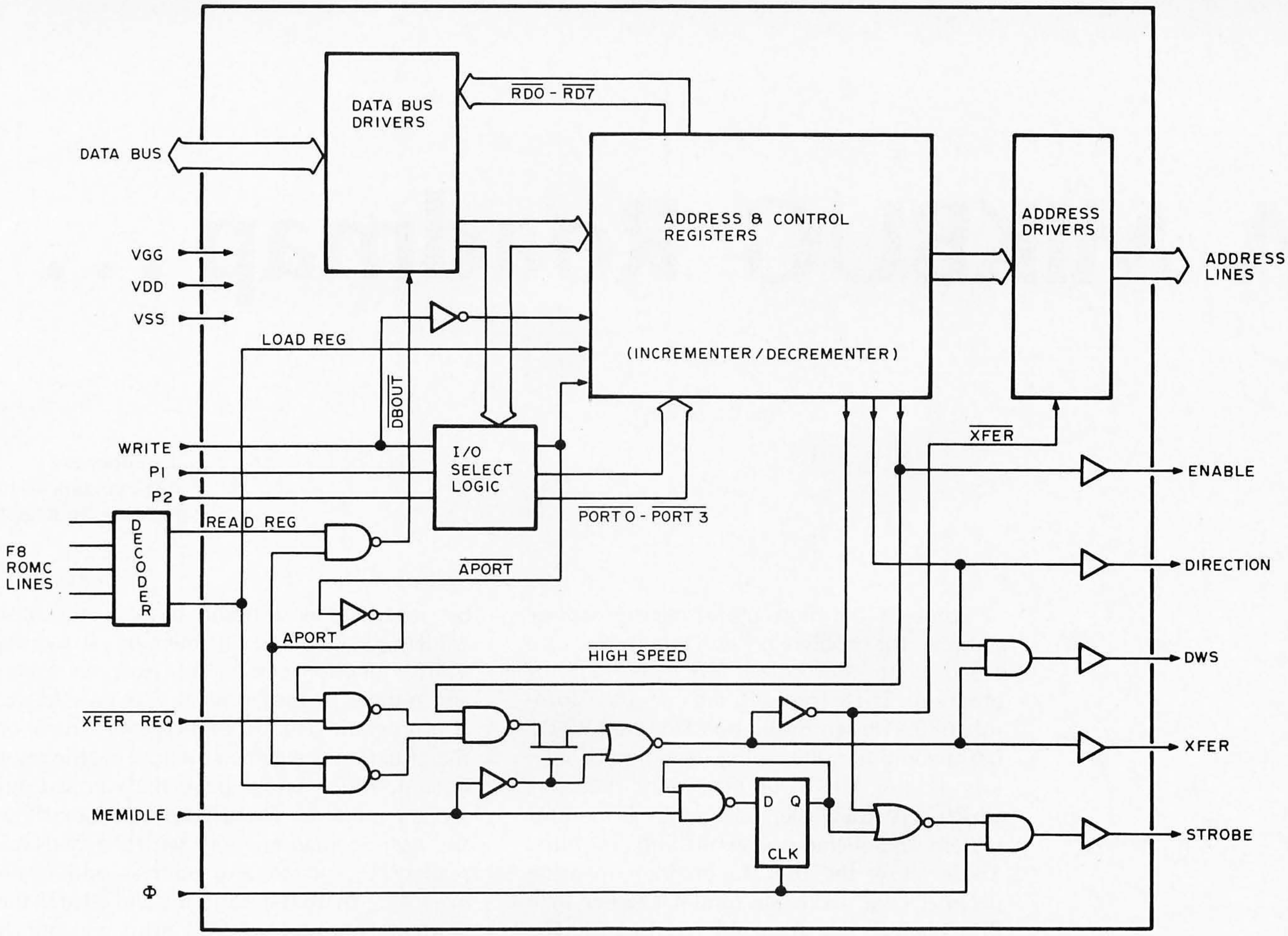


Figure 11: Block diagram of the 3854 direct memory access.

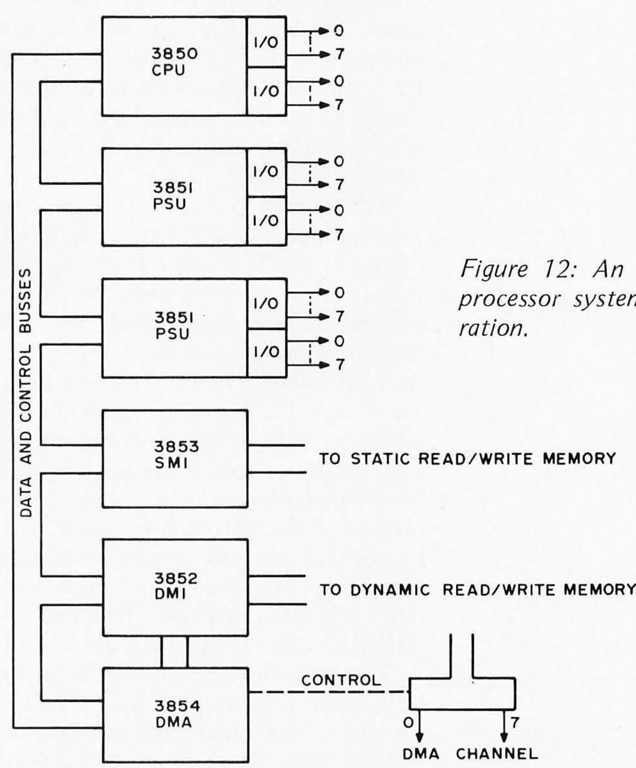


Figure 12: An F8 microprocessor system configuration.

development may be slightly more difficult or expensive for the hobbyist depending on the applications involved. By using a dynamic memory interface or a static memory interface along with standard memory chips, the more expensive program storage units may be avoided and make software development much easier. At least one program storage unit should, however, be included in a basic system to provide the additional IO and programmable timer ports. Ideally, this program storage unit would provide a standard, commercially available, software utility package designed for the average hobbyist. Additional units could then be added later for standard, more advanced software or when desired custom routines and programs have been thoroughly tested.

The F8 microprocessor system appears to be most ideally suited for mass produced microprocessor based products utilizing proven software. It does, however, provide enough flexibility to be of more than passing interest for general purpose personal computer applications.■

A MIKBUG Roadmap . . .

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Portland OR 97202

Some of the more useful microprocessor options for hobbyists available today are based upon Motorola's MIKBUG monitor program. These options include the Motorola 6800 Design Evaluation Kit, the SWTPC 6800 computer, etc. A big attraction of such kits is the MIKBUG read only memory, which provides the user with a monitor system and includes several utility routines. These allow the user to program in hexadecimal code from the terminal rather than in a binary code from the front panel. The purpose of this article is not to extol the virtues of the kit, but to demonstrate to proud new owners of 6800 systems that the MIKBUG read only memory can be used to much greater advantage than is generally pointed out by the manuals, particularly for IO techniques. An example of the use of MIKBUG routines is provided by the simple application of listing 1, a program which adds two numbers.

The MIKBUG firmware is a computer program for the 6800, copyright 1974 by Motorola Inc. It is called firmware because it resides in read only memory and is nonvolatile. In computers which use MIKBUG the program is located starting at hexadecimal address E000. The MIKBUG firmware takes 512 bytes, or just half of the 1 K memory. The program does not use the other half, nor does it use any device located at an address higher than hexadecimal E1FF, the end of the MIKBUG firmware. The 6800 microprocessor does use higher addresses for the interrupts and restart, but these are decoded to address locations within MIKBUG when MIKBUG is used.

The main function of MIKBUG firmware is to provide a monitor and several utility functions which make the programming and debugging processes easier. The monitor can be regarded as a home base in the vast wilderness of addressable memory. It accepts utility function commands, executes them, and returns to the terminal with an asterisk. If a program gets lost in memory, control of the situation is regained by pressing the reset button, which brings back the ever faithful servant monitor. The utility functions allow the user to load memory with a paper tape reader (L), go to any address and begin executing there (G), examine and change the contents of memory (M), print and punch selected blocks of memory (P), and display the contents of the stack, on which the values of all the registers are stored when under MIKBUG control.

To take advantage of MIKBUG one must have a terminal, and most often the beginning hobbyist will have no other peripherals to play with. Anyone who has purchased a microprocessor kit and has encountered the "let's see it do something" attitude from doubting friends and acquaintances will appreciate the immediate need for quick and easy IO techniques. Such techniques are present in MIKBUG, just waiting for the user, if he or she can find them. MIKBUG is organized in several groups of subroutines, which are selectively accessed by the MIKBUG utility functions that need them. For example, the memory change function needs a routine to input a character (M), output a character (space), input a 2 byte number (the address to be examined), input a carriage return, output a 2 byte number, space, then a 1 byte number, and so on. Many of these routines are nested several levels deep. For example, the routine to output a 2 byte number simply calls the routine to output a 1 byte number twice in a row. That's simple enough. Since a 1 byte number looks like two characters from the set zero through F

to the terminal, the routine to output 1 byte uses the routine to output a character twice. As you may have guessed, input routines for numbers and characters use the same cleverness. The point of all this is that the user can use aforementioned cleverness for his or her own IO routines by simply accessing the MIKBUG subroutines at the appropriate places. People with a MIKBUG listing, familiarity with the 6800 instruction set, and the time and patience to trace through Motorola's MIKBUG mouse maze of subroutines can figure out where the appropriate places are for themselves. I encourage you to attempt this, for your own edification and purification of spirit. (It's always a good practice, when learning a new computer's instruction set, to peruse a few existing programs like MIKBUG in order to get examples.) Those lacking one of the above ingredients, or the inclination to try it, can get some of the more useful information from what I've found.

Output Character

The output character routine, labeled OUTEEE in the MIKBUG listing, is located at hexadecimal address E1D1. It uses accumulator A as a data source. Thus you must define the contents of accumulator A which will then be interpreted as an ASCII character and shifted out in standard asynchronous format. It also uses accumulator B and the X register, but saves their contents at the beginning of the subroutine and restores them at the end. Therefore, the user need not be concerned with losing the contents of B or X. Listing 1 shows an example of the use of OUTEEE in a subroutine labeled PSTR which prints a string of characters, or a message. Control functions such as carriage return and line feed may also be implemented this way, by outputting their ASCII codes.

Input Character

The input character routine, labeled INEEE in the MIKBUG listing, is located at hexadecimal address E1AC. Like OUTEEE it saves the X and B registers. When accessed, INEEE loops while waiting for an asynchronous format character to be sent from the terminal, and upon receiving input, shifts data into the A accumulator. After access to INEEE the content of the A accumulator is the ASCII code for the key of the terminal which was pressed when INEEE was called.

Input Byte

This routine, labeled BYTE in the MIKBUG listing, is located at hexadecimal

Listing 1: This example program demonstrating the uses of MIKBUG uses all the techniques discussed in the article. The program requests and inputs two 1 byte numbers. It then adds them and prints the decimal adjusted result in an algebraic sentence. The program then asks the user if another run is desired. If the reply is Y, it branches to the beginning of the program; otherwise it returns to monitor. This program requires a mere 127 bytes of memory.

```
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        MOTOROLA M6800 CROSS ASSEMBLER, RELEASE 1.2

                         NAM    ADD
0000 8D 4A      BEGIN    BSR    CARRET    CARRIAGE RETURN
0002 CE 006D             LDX    #MESS1    START ADDRESS, 1ST MESS
0005 8D 52               BSR    PSTR      PRINT MESSAGE
0007 CE 0069             LDX    #MEM      START ADDRESS, MEM BLOCK
000A BD E055             JSR    $E055     INPUT 1ST NUMBER
000D A7 00               STA A  0,X       STORE 1ST NUMBER
000F 8D 3B               BSR    CARRET    CARRIAGE RETURN
0011 BD E055             JSR    $E055     INPUT 2ND NUMBER
0014 A7 01               STA A  1,X       STORE 2ND NUMBER
0016 AB 00               ADD A  0,X       ADD NUMBERS
0018 19                  DAA              DECIMAL ADJUST
0019 A7 02               STA A  2,X       STORE ANSWER
001B 25 48               BCS    OVRFLW    BRANCH IF ANSWER>99
001D 86 20               LDA A  #$20      SPACE
001F A7 03      ANSWR    STA A  3,X       STORE 1ST ANSWER DIGIT
0021 8D 29               BSR    CARRET    CARRIAGE RETURN
0023 BD E0BF             JSR    $E0BF     OUTPUT 1ST NUMBER
0026 86 2B               LDA A  #$2B      "+"
0028 BD E1D1             JSR    $E1D1     OUTPUT "+"
002B BD E0BF             JSR    $E0BF     OUTPUT 2ND NUMBER
002E 86 3D               LDA A  #$3D      "="
0030 BD E1D1             JSR    $E1D1     OUTPUT "="
0033 A6 01               LDA A  1,X       1ST ANSWER DIGIT
0035 BD E1D1             JSR    $E1D1     OUTPUT 1ST ANSWER DIGIT
0038 BD E0BF             JSR    $E0BF     OUTPUT ANSWER
003B 8D 0F               BSR    CARRET    CARRIAGE RETURN
003D CE 0078             LDX    #MESS2    START ADDRESS, 2ND MESS
0040 8D 17               BSR    PSTR      PRINT 2ND MESSAGE
0042 BD E1AC             JSR    $E1AC     INPUT CHARACTER
0045 81 59               CMP A  #$59      =Y?
0047 27 B7               BEQ    BEGIN     IF SO REPEAT PROGRAM
0049 7E E0E3             JMP    $E0E3     OTHERWISE RETURN TO MONITOR
004C 36         CARRET   PSH A            SAVE A
004D 86 0D               LDA A  #$0D      CARRIAGE RETURN
004F BD E1D1             JSR    $E1D1     OUTPUT CARRIAGE RETURN
0052 86 0A               LDA A  #$0A      LINE FEED
0054 BD E1D1             JSR    $E1D1     OUTPUT LINE FEED
0057 32                  PUL A            RESTORE A
0058 39                  RTS              BACK TO MAIN PROGRAM
0059 A6 00      PSTR     LDA A  X         GET CHARACTER
005B 4D                  TST A            BYTE=0?
005C 27 06               BEQ    EXIT      THEN GO BACK
005E BD E1D1             JSR    $E1D1     OTHERWISE OUTPUT CHARACTER
0061 08                  INX              NEXT CHARACTER
0062 20 F5               BRA    PSTR
0064 39         EXIT     RTS              RETURN TO MAIN PROGRAM
0065 86 31      OVRFLW   LDA A  #$31      "1"
0067 20 B6               BRA    ANSWR     RETURN TO MAIN PROGRAM
0069 0004       MEM      RMB    4         RESERVE 4 SPACES
006D 32         MESS1    FCC    8,2 NO.'S?
006E 20
006F 4E
0070 4F
0071 2E
0072 27
0073 53
0074 3F
0075 0D                  FCB    $0D,$0A,0
0076 0A
0077 00
0078 4D         MESS2    FCC    6,MORE?
0079 4F
007A 52
007B 45
007C 3F
007D 20
007E 00                  FCB    0
                         END

SYMBOL TABLE

BEGIN  0000  ANSWR  001F  CARRET 004C  PSTR   0059  EXIT   0064
OVRFLW 0065  MEM    0069  MESS1  006D  MESS2  0078
```

address E055. BYTE does not affect the X register, but unlike OUTEEE and INEEE, it destroys the previous contents of the B accumulator. BYTE uses INEEE twice to get two characters, checks to be sure they are hexadecimal characters, and combines them, converting them to a 1 byte binary number in the process. This is stored in the A accumulator and is present there on return from BYTE.

Output Byte

This routine, labeled OUT2H in the MIKBUG listing, is located at hexadecimal address E0BF. It outputs one byte of data located at some memory address chosen by the user. OUT2H requires that the X register be loaded with the address of the byte of data to be output, which may be located anywhere. This routine does not affect the contents of accumulator B, but does change the contents of accumulator A. It also increments the X register, which makes it very convenient for outputting sequentially located bytes in a block. More on this later.

Table 1: A descriptive list of the available MIKBUG subroutines summarizes the point of this article: Don't ignore the parts and pieces of your monitor, BASIC interpreter, compiler or other programs if you intend to write assembly language or machine language code. If you buy a program, ask for a source listing so you can get programming technique pointers. (Motorola is to be commended for handing out MIKBUG listings as a standard part of documentation right from the start. MIKBUG is described in detail in Engineering Note 100, "MCM6830L7 MIKBUG/MINBUG ROM," which was published by Motorola. The program is credited to Mike Wiles and Andre Felix of Motorola Semiconductor Products Inc.)

Entry Points Discussed Here...

Address	Name	Description
E1D1	OUTEEE	Character output: A sent to terminal device.
E1AC	INEEE	Character input: A set equal to next input character.
E055	BYTE	Hex byte input: input two characters as hexadecimal byte in A.
E0BF	OUT2H	Hex byte output: A sent to terminal as two hexadecimal digits.
E0E3	CONTRL	Return to MIKBUG control.

Other Useful MIKBUG Entry Points...

Address	Name	Description
E047	BADDR	Build address by calling BYTE twice; result in X register.
E067	OUTHL	Hexadecimal digit output from left nybble of byte in A.
E06B	OUTHR	Hexadecimal digit output from right nybble of byte in A.
E07B	PDATA2	Print string of data pointed to initially by X, until EOT character (hexadecimal 04) is found.
E0AA	INHEX	Input hexadecimal digit, on error go to CONTRL.
E0C8	OUT4HS	Output four hexadecimal characters and a space (uses OUT2H).
E0CA	OUT2HS	Output two hexadecimal characters and space (uses OUT2H).

Access to Subroutines

In the 6800 instruction set there are 16 branch instructions and two jump instructions. All may be used to access subroutines under certain conditions. The branch instructions all use relative addressing, which limits the range of branching from 126 bytes backwards to 129 bytes forwards. This is because they use a 1 byte operand as the branch offset. The jump instructions (extended addressing) use a 2 byte operand which allows them to jump anywhere. One of the branch instructions (BSR) and one of the jump instructions (JSR) store a return address in the stack before executing the branch. They go to the addresses specified by their operands and begin executing instructions at the new address until they encounter the return from subroutine instruction (RTS), at which point they return to the return addresses previously stored. Each return from subroutine instruction read by the processor must be paired with a branch or jump to subroutine instruction, although the same subroutine may be accessed by more than one branch or jump instruction. If a subroutine or a series of subroutines which is terminated with a return from subroutine instruction is accessed by any of the other branch or jump instructions, the return instruction will cause a return to an invalid address since the stack would not have been properly set up. Similarly, if a subroutine or a series of subroutines which does not end with the return instruction is accessed with jump or branch to subroutine, there will be no return to the main program. It just gets lost. The MIKBUG subroutines discussed in this article all eventually end with the return from subroutine instruction. Since they will always be located further than 129 bytes away from the main program departure point if called by a user, they must be accessed with the jump to subroutine instruction.

General IO Techniques

More often than not, a program will need to input or output more than one character or byte at a time. The use of subroutines which access the MIKBUG subroutines facilitate this. An obvious example is the need to print a message, which involves printing several characters in a row. A good way to do this is illustrated in the subroutine labeled PSTR in listing 1. PSTR requires that the X register contain the starting address of a block of characters to be printed. PSTR increments the X register each time it prints a character and returns when it encounters

an ASCII code of 00, which is a rarely used control character and is easily recognized with the test for zero (TST) instruction. Other stop characters could also be used. Similar subroutines may be used to input strings of characters or numbers. These subroutines may know when to quit by either counting the inputs and stopping at a preassigned number or by recognizing a stop character or number at the end of a string. A routine to output a string of sequentially located bytes would be even easier than PSTR using the same idea, because OUT2H increments the X register itself. Such a routine may also be terminated by either counting outputs or by recognizing a stop byte at the end of a data block. If a subroutine inputs or outputs hexadecimal numbers, it is best to count in order to terminate, otherwise one of the 256 possible numbers is excluded from use because it is the stop number. When using the decimal numbering system, any byte which is not a member of the set of 1 byte binary coded decimal numbers may be used as a stop byte.

Individual characters or small groups of characters which are input or output frequently in one program deserve their own subroutines. A good example is the combination of carriage return and line feed. The subroutine in listing 1 labeled CARRET illustrates this.

There may be times when an ouput is desired on certain conditions. There are 14 conditional branch instructions which make it easy for subroutines to serve these needs. The subroutine labeled OVRFLW in listing 1 illustrates this situation. In the sample program, if the decimal adjusted result of the addition is greater than 100, the carry bit is set and the byte reserved for the answer holds only the two least significant digits. OVRFLW is accessed if the carry bit is set, and prints a 1 in front of the answer byte to make the algebraic sentence correct.

Return to Monitor

A happy end to any program is a graceful return to monitor. This is labeled CONTRL in the MIKBUG listing, and is located at hexadecimal address E0E3. CONTRL should be accessed with the jump (JMP) instruction, and only at the end of the users program. Listing 1 includes examples of all the routines described above. Other routines, or different nesting levels of the ones mentioned here, may be found in the MIKBUG listing, and are summarized by name in table 1. The industrious reader can find routines which may be more useful to him or her, but the preceding ones will help get the show on the terminal.■

Classified Ads

WANTED: One set unpopulated MOD-8 PC boards and Monitor 8 extra RAM boards. Jerry Walker, 761 Clayton, San Francisco CA 94117.

WANTED: Parts to complete Teletype Corp model 35 for my own personal home computer system. I only have a typing unit. Karl F Kornafel, 2741 Baur Dr, Indianapolis IN 46220; home after 1800: (317)257-6044 or business after 2300: (317)262-2445.

WANTED: Schematics or PC board layout for simple Intel 8008 microprocessor using minimum hardware; also need simple 1702A PROM programmer schematic. Will pay or exchange for technical information. Raymond J Ramirez, 2A-8 Bairoa Pk, Caguas PR 00625.

FOR LEASE: Model 735 Silent 700 portable data terminal. 6 month term for $90 per month. Has an acoustic coupler, RS 232 interface, full or half duplex, 10 to 30 cps, ASCII code. Dick Harding, 633 Kingwood Rd, King of Prussia PA 19406; (215)265-3719 (eve) (215)864-7017 (day).

WANTED TO BUY: PDP8-E expander box with cable and quad slot bus assembly. 861-C cabinet power control, MI8-E bootstrap, MM8-E and MM8-EJ memory modules, card reader, printer, disk control and drive, magnetic tape, cassette system, all with cable and interface card for PDP8-E. Willing to talk about any PDP8-E hardware or software. Please call: (617)861-6500 or write: Harry Bellmar, Minuteman Regional School, 758 Marrett Rd, Lexington MA 02173.

FOR SALE: FLEXOWRITER model SPD has 8 level reader and punch. Previously used to create computer data base. Standard unit without modifications or changes. $175. M T Buckelew, POB 10, Falls Church VA 22046.

FOR SALE: Memories – 270 1103 1 K RAMs $400, 160 74S206 256 bit RAMs $500, and a core stack constructed from 17 planes of IBM 1401 memory $200. Each plane of the stack is arranged as a 50 x 80 matrix with separate sense and inhibit lines (68,000 bits total). All of the above will be sold with documentation included. Also for sale – 8080A CPU chip $25. Contact: Arthur W Wetzel, 222 North Craig St, Apt 2A, Pittsburgh PA 15213, (412)624-5208 (day) or (412)683-6293 (evening).

WANTED: Information on care and maintenance of a Friden 2303 Flexowriter. Also would like information on how to interface it with a processor. I will pay for cost of duplication and mailing. Dan Hastings, 5055 Lily La, Apt 210, Indianapolis IN 46254, (317) 297-1079 (call collect).

Readers who have equipment, software or other items to buy, sell or swap should send in a clearly typed notice to that effect. To be considered for publication, an advertisement should be clearly noncommercial, typed double spaced on plain white paper, and include complete name and address information. These notices are free of charge and will be printed one time only on a space available basis. Insertions should be limited to 100 words or less. Notices can be accepted from individuals or bona fide computer users clubs only. We can engage in no correspondence on these and your confirmation of placement is appearance in an issue of BYTE.

Please note that it may take three or four months for an ad to appear in the magazine. ■

FOR SALE: Tektronix model 115 pulse generator, 10 ns pulser with delay and 100 Hz to 10 MHz repetition with manual, like new, $595. Tom Murph, 4244 Philadelphia Dr, Dayton OH 45405, (513) 274-4405.

FOR SALE: Programs in BASIC, including games, scientific and educational programs. Also program guides and software packages. I have written a number of programs which I will sell for $1 to $5. All programs come with complete documentation including a cross reference listing of all variables. For list, send stamped envelope to: Richard Traynham, 2928 Softwind Trail, Fort Worth TX 76116.

DEC:BUY,SELL,or TRADE: I have some DEC-11 modules and hardware. Included are such things as a DF11a, M7821, M795, and some brand new W9671 PDP-8 Wire Wrap Boards. I need, or am interested in, the following items: DL11e, DF01 or other modem, DR11c, KE11, KW11L, TA11, RC11, or a floppy drive. If you can part with any of the aforementioned items for cash or trade, please let me know. L Stewart, 1402 Regent St, Apt 506, Madison WI 53711, (608) 255-5380.

FOR SALE: 1 C-Mod 80 system including: CPU (with 5204 Micro-Monitor), 2 K RAM card (2102-1's), parallel or serial IO card, backplane with connectors for 12 cards, $150 for above. RCA CDS 1200 modem with documentation, $50; Teletype model BRPEB8 high speed 8 level punch, $45; RPC-4000 Computer System (has Fortran), $500. Call Sam Ulin at (302) 475-7355 evenings or write POB 216, Claymont, DE 19703.

HELP: Does anyone out there have any information on a Data Trends Inc general terminal unit? I need schematics, operating information, anything I can get. Also need any data on International Computer Products Digi-Deck units. I will pay all reproduction costs and shipping, or I have wall sized (11 X 14) IC microphotos and electronics graphics—trade? Contact: Bob Retelle, 2005 Whittaker Rd, Ypsilanti MI 48197.

FOR SALE: DEC PDP-8s, 4 K core memory, serial interface, possible IO bus, all cables and power supplies. $450 or best offer or will trade for video terminal, 8080 machine, or any DEC mass storage peripherals. Also needed: information on Design Elements or Mg2 Data Systems modem, model 88-OA. Jim Gonzalez, 150 S Summit Av, Hackensack NJ 07601, (201)342-3110.

WANTED: BYTE issues November 75 and April, May, June 76. Will pay almost any price. George Valaitis, 647 Linkfield Rd, Watertown CT 06795, (203)274-5628.

HELP: Neophyte will pay for technical assistance in converting Burroughs TM20K714 terminal, with or without the control unit, to something my IMSAI 8 K BASIC can digest. Have 7 data bits in parallel at the terminal, no parity or buffers. I want to send entire line with a carriage return. A semischematic would do. Leo Biese, RFD 1, Hill NH 03243, (603)744-8906.

FOR SALE: VIATRON 2111 data management system (as advertised in March 1976 BYTE, page 87). The unit is in brand new condition and works like a charm. Complete with instruction manuals, cassettes, and schematics for $400; also IBM Selectric Printing Robot attachment for above $175. you pay shipping (160 lbs). First cashier's check or money order for $550 takes them both. Bill Robertson, 123 W Pearl St, Apt 22, Nashua NH 03060.

FOR SALE: Cleaning house, all new unused parts. Intel 4004 $5; 4040 $10; 4289 $2; 4201, 4002-1, 4003 $1 each; MC6871A $5; MC14411 $3; 1MHZ xtal $1; 1.797 MHZ xtal $1; MOS TECH scientific calculator chip set 2525-2526 with data sheets $5. Ron Angstadt, RD 3, POB 281, Kutztown PA 19530.

WANTED: Does anyone have a spare copy of *SWTP Newsletter* No. 1? It's no longer available from *SWTP*; many thanks!! Also, if you have use for an IBM 6400 accounting system, please write: "Pete" Peters, Microputer Tinkers Society, 3845 Le Bleu St, Beaumont TX 77707.

FOR SALE: ASR33, excellent condition (used by a little old Altair), $800. George Nelms, 3908 Abbott Av S, Minneapolis MN 55410, (612) 922-3087.

FOR SALE: Altair compatible 8080 CPU board with sockets, $35. CDC floppy disc drive in a sack includes spares and documentation, $125. Super Display: Computek 400/20, 96 character ASCII, Vector and Curve generator, Joystick input and keyboard, RS 232 110-2400 baud, full documentation, $1250. Vermont Research Drum, 950 tracks, 2600rpm, Read/Write electronics, documentation, $350. Hans Mahr, 28028 Ella Rd, Rancho Palos Verdes CA 90274, (213) 377-0735, eves.

FOR SALE: Paper Tape Splices. Prepunched, clear or opaque mylar patches for 8 channel tape. $2 per 50 or $3 per 100. Send SASE. Finest quality, money back guarantee. Mike Campo, 457 Promontory Dr W, Newport Beach CA 92660, (714) 751-8271.

FOR SALE: Dual-drive Innovex Diskette (1974) for PDP-8E, ready to plug into Positive I/O Interface. Includes test tape, 10 used Diskettes (some with glitches), my own handler, 48 tracks, 8 sectors of 259 12 bit words per sector. Best offer that is not absolutely ridiculous. William T Powers, 1138 Whitfield Rd, Northbrook IL 60062.

FOR SALE: Ampex core memory 32 K of 8 bits, 300 ns access with R/W electronics, power supply, and complete manual. $750 or make offer. Rainer McCown, 9537 Longlook Ln, Columbia MD 21045.

WANTED: Information leading to the contact of Charles D Hackett, former USAF 306X0, current electronics freak. Have him contact Ssgt James D Tucker, Lot 8, Hughes Trlr Crt, Knob Noster MO 65336, (816) 563-2177, after duty hours.

COMPUTING MACHINERY FOR SALE: One KIM board modified for half duplex terminal (can easily be changed back) in good working order with complete documentation. Also one JOLT system with CPU board, PROM board (with one PROM)and power supply mounted in box. Something wrong with power supply but otherwise in working condition. Will sell both together for $200 or KIM for $150 and JOLT for $75 all as is. Norman Bringsjord, 1346 Connecticut Av NW, Washington DC 20036, (202)785-9440.

WILL TRADE/SELL: KELSEY 8 by 10 letterpress (like new) with 10 trays of type, (6 pt to 36 pt). All will be included. To use for business or hobby. Lots of extras. Value $750. Also have Thomas-Paramount Heathkit electronic organ in 100% mint condition with bench value $1150. Want microcomputer ensemble (IMSAI, MITS, ALTAIR, SWPTC, etc). Can be kit (unassembled) or assembled. Write or call and tell me what you have. Shipping arrangements will be negotiated to interested parties. H Zallen, PO Drawer 2790, Norman OK 73070, (405)364-1119.

REALITY STRIKES!: I'm sitting on more of a system than I need in my work. 16 K PDP-8F (8 K core), dual Innovex diskette, VT-8E alpha/graphic terminal and KB, ASR-33 TTY, 16 channel A/D, 2 channel D/A in need of two D/A converter ICs, rolling cabinet with 3 hinged sides. Worth over $13 k new; everything works. Will settle for less than half price, and accept some items in trade (toward Z-80 system) in lieu of cash. See your bank and make me an offer. William T Powers, 1138 Whitfield Rd, Northbrook IL 60062, (312)272-2731.

FOR SALE: Motorola Evaluation Board 2 with Minibug 2 ROM, crystal clock, baud rate generator from 75 – 9600 baud. Has serial interface for 20 mA TTY and RS 232 output, two 8 bit parallel output ports and fully buffered address and data lines. PC board has sockets for all chips and a socket for PC edge connectors. Asking $350 or best offer. R C Brand, 62 Preston Dr, N Kingstown RI 02852, (401)295-1996 (evenings).

WANTED: BYTE back issues, 2, 3, 8, 9 and 10. No reasonable offer refused, and I will accept Xerox copies. Write Mark Brown, Minneapolis Medical Research Foundation, 501 Park Av, Minneapolis MN 55415.

Product Description

Put Your Computer to Work



Bill Roch
RO-CHE Systems
7101 Mammoth Av
Van Nuys CA 91405

Now that you have your hobby computer assembled and running . . . what next? Well, there is always Star Trek, Life, Hunt the Wumpos, and more in the way of computer games. After the games maybe you built a Christmas card list, list of anniversaries, phone directory or the like. But what happened when you volunteered to keep the batting averages for the Little League? All of a sudden you ran out of memory or you had to reenter the file of data each time you did an update.

It seems the manufacturers of our little "beasties" did not foresee the need to read and write records. Sure, you can save and load blocks of data, but what about that collection of characters which makes up fields and a group of fields which makes up records?

Our new product (RO-CHE Systems) is a controller designed to handle multiple motor control of audio cassette drives using status bits controlled by the computer. The software we supply with the unit is designed to work with either the high speed Tarbell cassette interface or the Altair 8800 ACR interface. In the past it took a commercial system or time sharing house to give you the ability to handle files containing individual records. With the "Magic Black Box" as we call it, control of audio cassette motors provides an element of automation previously unobtainable using simpler cassette interface disciplines. We grabbed the extra status bits available on Don Tarbell's cassette interface and used them as control signals for the multicassette controller. In using our control box with other cassette interfaces, all you need to supply, outside of software patches to the driver routines, is a parallel interface output to accomplish the same function.

This controller handles up to four inexpensive cassette recorders at one time without losing the ability to save and load from Altair BASIC and other packages. The software developed with our unit reads and writes physical records to and from software selected records. It's like having a big computer with four tape drives but not as fast.

With all this file handling software and the hardware control box available at a fraction of the cost of a big system, how can it be used?

Personal computer users are doctors, lawyers and indian chiefs, butchers, bakers, candlestick makers, white collar, blue collar and dirty collar workers who are members of lodges, churches and bowling leagues, and owners and managers of businesses.

With the capability of handling data files larger than your memory size, it becomes only a matter of user application software to create such things as:

- Mailing lists
- Membership rosters
- Inventory
- Accounts receivable
- Accounts payable
- Back orders
- Batting and bowling averages
- Form letters
- Word processing
- Check book balancing
- Income tax calculations

(I've started . . . you add to the list)

We demonstrated the multicassette controller at the June and July Southern California Computer Society meetings where it was set up to create a mailing list.

The demonstration started by one individual keying in his name and address which were written on deck 0. The next individual entered his last name. The software read the name from deck 0 and decided which name to write to deck 1 first. The rest of the name was entered and now the tape in deck 1 had two names and addresses. Each time a name was entered, the old master file was read and the new name was merged in alphabetically

to the new master file. The demo software also had the ability to find a last name and print it out or to list the whole file of names. Last names were used as the key field for identification, but it could just as well have been part numbers, account numbers or any other such identification code.

In addition to the cassette IO routines, the software supplied with this box contains a number of utility routines for such things as keyboard entry and echo, message output, string compare, line feed, carriage return, string moving, etc.

Where to Get It

RO-CHE Systems, 7101 Mammoth Av, Van Nuys CA 91405, offers the multi-cassette controls in a two and four port model at $95 and $125 in kit form, and $135 and $175 when assembled and tested. A two port add on kit is also available at $32. Shipping and handling is $2.50 per unit except the add on kit which is $1.

The units come complete with assembly and operating instructions and a cassette containing the RCSCOS operating systems, Tarbell IO and a low core assembler editor and monitor. Source listings of the operating system are available at $5 each.■

Calculator Keyboard Input for the Microcomputer

Joseph Hoegerl
RD 1 Box 262
Guy Mills PA 16327

There was a need for a simpler method to put programs into memory.

Some months ago I purchased an RGS Electronics 008A Microcomputer Kit in order to learn about this computer thing. In the intervening months it has served a number of very useful functions.

First, I learned about the basics of computers. In putting the kit together, I learned a great deal about the 8008 microprocesser and its associated circuits. By solving a problem in the operation of IO transfer, I got to understand a lot about the logic of my computer. (It turned out to be a malfunctioning 7442 chip which provided the IO gating pulses.)

Second, I have become reasonably proficient in programming, using the basic machine language of the 8008 in octal form. The instruction set of the 8008 is simple enough that one can remember the numbers in octal from about as easily as the mnemonics and it saves time when working with shorter programs.

Third, it has provided me with a number of projects involving the computer itself or with the equipment tied into it.

It did not take long for me to see that entering programs by way of the front panel switches was tedious and time consuming, especially since programs quickly become more complicated and longer as programming proficiency develops. There was a need for a simpler method to put the programs into the memory. The thought occurred to me that an inexpensive and simple solution might be to adapt a calculator keyboard to enter data in octal form. The circuit described in this article is the result of thinking about this alternative. The unit proved to be both trouble and error free in the five months since it was completed. I use the keyboard continually, even though I have since interfaced a Model 15 Teletype and a five level tape unit to the CPU which enables entering programs from tape.

A bootstrap program for initial input after a power shutdown requires only 15 bytes which must be entered by the original front panel switches (see listing 1). The main program requires only 62 bytes and these are entered using the bootstrap (see listing 2). The keyboard has provision for entering data either in octal or hexadecimal format. The unit may be built with the full capability, or parts can be omitted to dedicate the key-

Listing 1: Bootstrap Keyboard Input Program. This 8008 program reads the keyboard device of figure 1 and loads memory in ascending sequence. Its primary purpose is to enter the second full program of listing 2.

Intelese Octal Address	Octal Code	Label	Op	Operand	Commentary
000/000	006 070		LAI	070	define device address;
000/002	161		OUT		select device;
000/003	056 XXX		LHI	(H)	load upper address byte here;
000/005	066 XXX		LLI	(L)	load lower address byte here;
000/007	300		LAA		no op;
000/010	250		XRA		clear "A" to zero;
000/011	141		OUT		send control pulse out to interface;
000/012	101		INP		read a byte into accumulator;
000/013	370		LMA		load the byte into memory;
000/014	060		INL		increment the address pointer;
000/015	121		OUT		output a pulse to reset data ready flag;
000/016	000		HLT		end of program, wait for restart.

board to octal or hexadecimal input exclusively.

Circuit Description

The circuit of the input device is given in figure 1. A diode matrix decodes the key-switch closures into binary format. Data is entered in the normal sequence with the most significant digit first. The three 7475 latches are activated sequentially (only two are used for the hexadecimal mode of input) and the binary equivalent of each digit is held in the 7475 latches until read by the computer and then cleared by a signal from the computer, or, in case of keypressing errors, by pressing the clear entry (CE) key on the keyboard.

The choice of octal or hexadecimal is accomplished by the use of two 74157 multiplexers, IC11 and IC12. These are set to pick hexadecimal or octal encoding by S1. If only octal format is needed, the binary data can be taken directly from IC1, IC2 and IC3, at the points marked A0 to A7 on figure 1. If only hexadecimal format is desired, IC11, IC12, and IC3 may be omitted and the outputs taken from the remaining IC1 and IC2 at the points marked B0 to B7 on the diagram.

The circuit operates as follows: When a key is depressed, one or more of the five decode lines will go to the high state. (Four lines are used for encoding the digits 'I' to 'F'; and the fifth line is used to decode the zero key.) These are inverted by the five inverters, IC4A through IC4E, the outputs of which go low when a key is pressed. This causes the output of IC5, which functions as a nor gate, to go high. This transition is converted to a positive going pulse by the combination of IC4F, capacitor C1 and resistor R6. The pulse is inverted and squared off by IC6D. The output pulse of IC6D is fed to the three gates IC10A, B and C, one of which is enabled by the state of the 2 bit counter IC7A and IC7B. A "clear flag" signal from the CPU, or a clear entry (CE) key closure will reset the two flip flops

Toggle switches are relics of the dark ages (of computing).

Listing 2: Full Keyboard Input Program. This 8008 program defines a memory address with the first two bytes read from the keyboard after restart. Then it enters a loop which loads memory byte by byte in ascending address sequence.

Intelese Octal Address	Octal Code	Label	Op	Operand	Commentary
000/070	006 070	START:	LAI	070	load address of keyboard;
000/072	161		OUT		select device;
000/073	121		OUT		reset flag;
000/074	106 116 000		CAL	DATA	A:=keyboard input;
000/077	350		LHA		loads upper address into H;
000/100	106 116 000		CAL	DATA	A:=keyboard input;
000/103	360		LDA		loads lower address into L;
000/104	106 116 000	MBYTE:	CAL	DATA	A:=keyboard input;
000/107	370		LMA		put byte into memory;
000/110	106 162 000		CAL	INHL	to increment H and L;
000/113	104 104 000		JMP	MBYTE	repeat for each byte in turn;
000/116	006 200	DATA:	LAI	200	set multiplexer to status;
000/120	141		OUT		status pulse;
000/121	016 002		LBI	2	set counter for debounce routine;
000/123	101	FLOOP:	INP		input flag status;
000/124	044 200		NDI	200B	mask flag bit;
000/126	022		RAL		put flag bit into carry and check carry bit;
000/127	100 123 000		JFC	FLOOP	if carry false, then check again.
000/132	011		DCB		if carry true then delay, then check again;
000/133	110 143 000		JFZ	DLY	22 ms delay;
000/136	250		XRA		clear accumulator and carry;
000/137	141		OUT		set multiplexer to accept data;
000/140	101		INP		accept data into A;
000/141	121		OUT		send out reset pulse;
000/142	007		RET		end of FLOOP routine;
000/143	106 151 000	DLY:	CAL	DELAY	22 ms delay;
000/146	104 123 000		JMP	FLOOP	try again;
000/151	036 326	DELAY:	LDI	326	set counter to give 22 ms delay;
000/153	300	TIME:	LAA		waste time;
000/154	300		LAA		waste more time;
000/155	031		DCD		decrement counter;
000/156	110 153 000		JFZ	TIME	waste time until counter is zero;
000/161	007		RET		return to calling program;
000/162	060	INHL:	INL		increment lower address;
000/163	013		RFZ		return if lower address not zero;
000/164	050		INH		increment upper address if lower was zero;
000/165	007		RET		return to calling program;

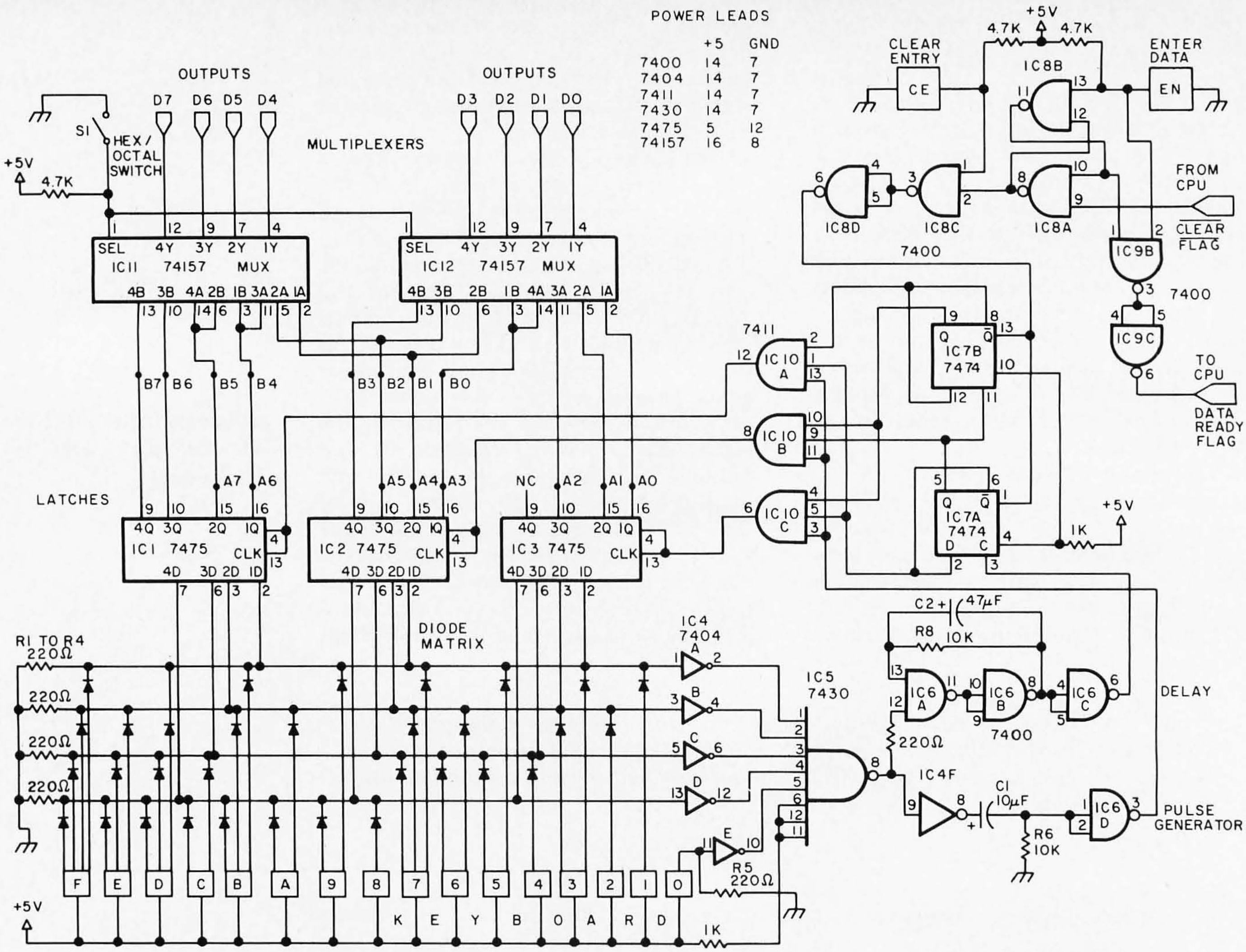


Figure 1: Keyboard Input Logic. This circuit contains a diode matrix which encodes 16 hexadecimal input keys as a four bit code, a register to contain the results of that conversion, a multiplexer which gives a switch selected 3 digit octal or a 2 digit hexadecimal interpretation to the inputs, and control logic for keyboard debouncing, clearing, and entering data.

to the start position. When this happens, gate IC10A will be enabled by a high level on two of the three inputs. The pulse from IC6D mentioned previously then satisfies the gate and its output will go high, momentarily causing IC1 to latch on the data present on the decode lines.

When the key initially depressed is released, the delay monostable made up of R7, R8, C2, IC6A, B, and C, causes a pulse which increments the counter formed by flip flops IC7A and B, thus setting up two lines of IC10B to a high level and ready to accept the next digit. Note that this does not happen until the key is released, thus avoiding erroneous writing of the same data into more than one latch. This process continues for the third digit with IC10C enabled.

After the desired digits have been entered on the keyboard, the enter (EN) key is pressed. This sets the flag RS flip flop made up of IC8A and B. To prevent multiple data entry, its output must pass through the dual input gate IC9B, which will prevent data from passing through until the enter key has been released. At that time a high level will appear on the data ready flag output, signalling the CPU that data is ready for processing. The RS flip flop is reset by a negative going pulse on the clear flag input from the CPU. When this flag flip flop was initially set by the enter key, the 7474 flip flops IC7A and B are cleared to zero through IC8C and D.

The Interface

A standard RGS Electronics interface board was used with the addition of the

circuit shown in figure 2. This circuit is a multiplexer which allows one of the eight data bus lines to read either data or the data ready flag output. To simplify programming, D7 was chosen for the dual purpose line.

The instruction "LAI 200" followed by a 141 output control instruction will set the Q output of IC13A to a high level. This will set the multiplexer IC14 to accept data from the data ready flag on the D7 input, signalling the CPU that data is available. The program then performs an XRA which clears D7 to zero, followed by a 141 output control instruction which sets the Q output of IC13A to a zero and the $\overline{Q}$ to a high level which switches the selector of IC14A, B and C to accept the D7 output of the 74157 IC11.

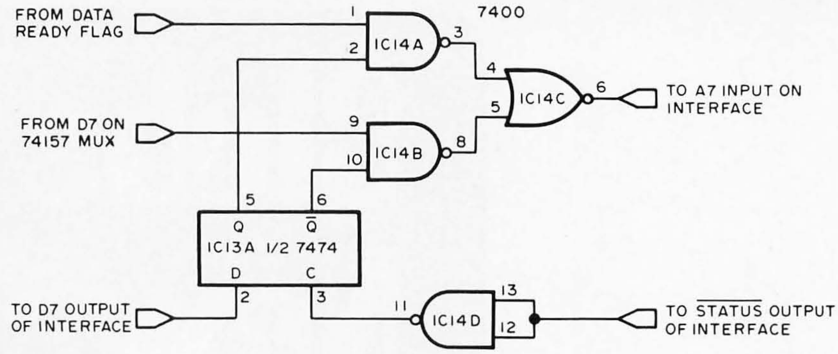


Figure 2: RGS-008A Interface Logic. This diagram shows the logic used to control the interface to the author's RGS-008A computer.

Construction Notes

Little trouble was encountered in the construction of this unit. The circuit, with the exception of the keyboard and the interface, was all put on a single sided printed circuit board four by six inches. As I do in most of my construction projects, I used single sided board and wired across the board where I couldn't paint in the required wiring. I have found that this technique gives results with considerable saving in time when only one model is to be made. Ribbon wire was used between the circuit and the keyboard. This allowed the keyboard to be moved around to the most convenient location and out of the way when not in use. Power was taken from the power supply of the computer, which is capable of supplying three amperes. My present memory size is low enough to make a considerable excess power available for peripherals. The universal interface board supplied by RGS Electronics in kit form is a very flexible circuit which lends itself to many types of external equipment such as this unit.

Programming

A bootstrap program, 15 bytes in length, is found in listing 1. It is placed into the first 15 address locations on page zero to take advantage of the RST instructions to minimize program length. These bytes must be entered using the original switches on the front panel of the CPU. The purpose of the simple bootstrap program is to load a second, more sophisticated bootstrap program.

The starting address of the program to be entered is placed in location 004 for the upper and 006 for the lower address. These two addresses are two of the 15 bytes which make up the program. Operation is as follows:

1. Set the front panel switches to 005B.
2. Press the "clear entry" key on the keyboard.
3. Enter the three octal numbers that represent the program byte.
4. Press the enter (EN) key.
5. Press Interrupt on the CPU front panel.
6. After the first byte has been entered, set the front panel switches on the CPU to octal 015, then repeat steps 3,4, and 5 above for each additional byte to be entered.

You will note that this is not a continuously executing program but stops after each entry and is restarted for each byte using the RST and interrupt instruction.

A More Sophisticated Bootstrap Program

Listing 2 shows a program which requires only 62 bytes and is entered using the simple bootstrap program. In my case the program is located at page zero, octal location 070. It is a continuously executing program and after finishing program entry, the front panel switches are set to zero and an interrupt entered. It operates as follows:

1. Set the front panel switches to 075 and press interrupt switch.
2. Clear the keyboard with the clear entry (CE) key.
3. Enter the upper starting address and press the enter (EN) key.
4. Enter the lower address and press the enter key.
5. Enter the program bytes, sequentially, pressing the enter key for each byte. If more than one byte of the same program instruction is to be put into memory, it is not necessary to rekey them. Merely press the enter key again for each additional byte. ■

Clubs and Newsletters

The RAMS of Rochester

We recently received word from Dave Noderer, secretary of the Rochester NY Area Microcomputer Society, a relatively new organization, that meetings are scheduled for the second Thursday of each month at the Rochester Institute of Technology, Building 6, Room 1030 at 7:30 PM.

The primary objectives of RAMS are exchanging newsletters, establishing group purchasing power, and organizing regional computerfests and conferences. A monthly newsletter called *Memory Pages* is published and can be obtained by writing to RAMS, POB D, Rochester NY 14609.

Omaha Hackers – Getting It Together

Mid-America Computer Hobbyists announce the organization of an Omaha based club primarily to exchange information on construction and software development projects. Those interested in joining MACH should get in touch with Lt Tom Smith, 2708 Calhoun St, Bellevue NE 68005.

British Columbia Computer Society

A group of computer hobbyists have banded together in British Columbia. For more information about what should be a promising new club contact Karl Brackhaus, 203-1625 W 13 Av, Vancouver BC Canada V6J 269, (604) 738-9341.

San Diego Computer Society – Personal Systems

SDCS has apparently developed into a first rate organization at least by the looks of its newsletter, *Personal Systems*. Among the articles in the October issue (the latest we have unfortunately) is one by C S Pepper, "The MM5740AAE Encoder," a complete keyboard interface system capable of encoding 90 switch enclosures in a ASR 33 Teletype format as a 9 bit code, "The Micro-Tower" by Dr Lance Leventhal, the next few articles of which will deal with computer intersection sets, and an article on an "Extended Debugging Aid" by Richard S Mason. All major entries in this newsletter appear to be technically competent and thorough. So, if you want to learn more about computers write *Personal Systems*, San Diego Computer Society, POB 9988, San Diego CA 92109.

New England Computer Society

NECS continues to publish a fine monthly newsletter, *The COMPUTERIST*. Volume 1, Number 1, featured an article on the future of the home terminal: a feedback loop with the potential to plug personal experience in the form of coded brainwaves into any conceivable sequence or situation. According to author Joel Henkle of The Valley Institute, Hillsboro NH, this could become a form of "electronic LSD." So watch out; this could have some very interesting possibilities!

Along with the fine articles which appear here monthly is a rundown on the happenings of six hobbyist groups in the region. This is a mighty handy journal for New England hackers. Subscription rate is $6 per year. Write POB 3, South Chelmsford MA 01824, or call (617) 256-3649.

Northwest Computer Club

It looks like some noteworthy things are happening in the Seattle area through the Northwest Computer Club. An interesting newsletter has been assembled: a monthly presentation of computer lore and a fairly extensive classified section that might help a body save a buck or two. The October issue features an article called "8080 Programing

Tips and Tricks," some nifty ways to use the unique address calculation ability on this machine. There's also some information on the West Coast Computer Faire, April 15 to 17, at the San Francisco Civic Auditorium. Contact the Northwest Computer Club at POB 5304, Seattle WA 98105.

Rock Island Hackers Unite!

The Quad City Computer Club in Rock Island IL held its first meeting on October 24. A group of thirty got together for a presentation. To contact what may be an up and coming club write: John E Greve, 4211½ 7th Av, Rock Island IL 61201.

KC Thru Put

The Computer Network of Kansas City has been publishing a newsletter called *KC Thru Put*. If you'd like to get in touch with the folks in Kansas City, send a note to *KC Thru Put*, 968 Kansas Av, Kansas City KS 66105.

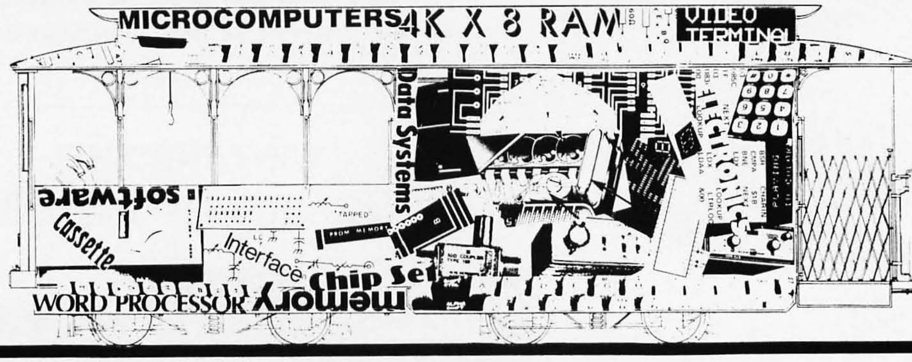
Central Florida – A New Club

Christian S Bauer, assistant professor of engineering at Florida Technological University in Orlando, announces the formation of a microcomputer club open to the community as well as students. The plan is to undertake construction projects from BYTE and a number of Motorola 6800 designer's kits in order to build up a microcomputer center. Contact Dr Bauer at (305) 678-2413 to find out more.

PACE Users Group?

"We are seeking to form a PACE users group for the purpose of exchanging software, describing systems implementations, and communicating hardware hints and kinks on interfacing peripherals to the 16 bit National Semiconductor microprocessor. Although National Semiconductor has its own microprocessor users' society, this organization covers IMP16 and SC/MP as well, and is also not primarily hobbyist oriented. Our intention is to serve as a clearing house for PACE based systems, both homebrew and commercial kit configurations (such as PACER), which will bring existing and potential users together to share ideas, know-how, and the pleasures and pains of getting a system up and running. Up the 16 bit microprocessor!

"Please send your name, address, phone number and a brief note on your system and its application to me, Jock Millenson, at 64 The Uplands, Berkeley CA 94705."■



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- As the Coordinator/Moderator

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- Speakers & Panel Participants
- Interesting Exhibits (homebrewed or commercial)
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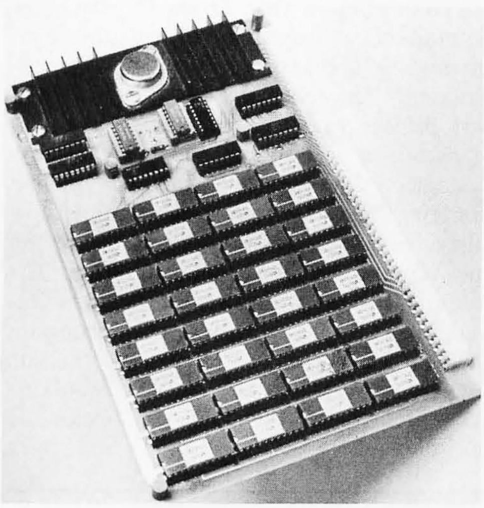
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- Speech Synthesis Using Home Computers
- Computers & Amateur Radio
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- Program & Data Input via Optical Scanning
- Floppy Disc Systems for Personal Computers
- Computer Games: Alphanumeric & Graphic
- Computers & Systems for Very Small Businesses
- Personal Computers for the Physically Handicapped
- Personal Word-Processing Systems
- Software Design: Modularity & Portability
- Personal Computers for Education associated with a Univ. of California short-course
- Several Sections Concerning Standards
- Other Sections for Club Leaders, Editors, Organizers, etc.

▪ **Co-Sponsors** include amateur, professional, & educational groups:
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  Southern California Computer Society
- Both Area Chapters of the Association for Computing Machinery
  San Francisco Peninsula Chapter
  Golden Gate Chapter
- Stanford University's Electrical Engineering Department
- Community Computer Center
- People's Computer Company

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What's New?

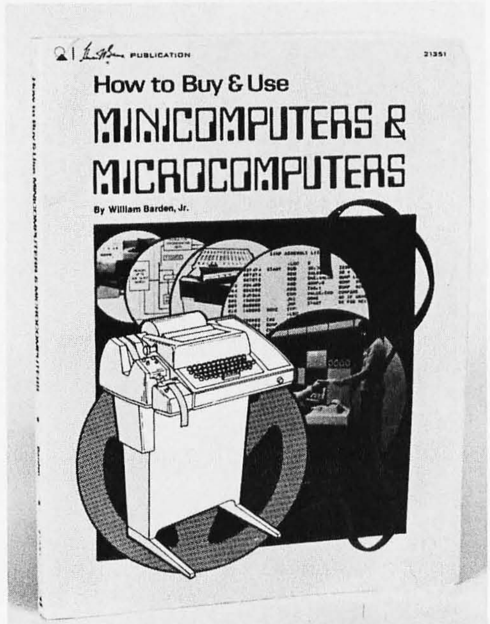


A New Case of Independent Suppliers

For some time now, the small computer world has been treating the Altair bus of MITS as the de facto bus to interface if you're about to make an independent peripheral or processor. Well, sales of the Southwest Technical Products Corporation 6800 system have apparently gotten to the level where at least one company feels there are enough of them about to supply an independent peripheral product. This product, the first we've seen for a 6800 by Southwest, is the M-16 16 K memory board by Smoke Signal Broadcasting. It uses the new AMD 9141 ADC static memory chips and costs $595 and delivery is quoted as from stock. With the SWTPC 6800 it is now possible to expand to 32 K without any modifications of the circuitry by simply plugging in two of these boards, and you can go all the way to 48 K with some rewiring of the SWTPC 6800 processor to avoid conflicts between MIKBUG and addresses 8000 to BFFF hexadecimal. This product is the first of several the company has designed and plans to produce which will plug into the SWTPC computer. The size of this board is the same as the SWTPC 6800 processor board (5.5 by 9 inches; (14 cm by 23 cm) and the 9141 chips utilized are fast enough to run the 6800 at its full rated speed.

Contact Smoke Signal Broadcasting at POB 2017, Hollywood CA 90028.■

So You Want a Beginner's Introduction? Try This Book as a Starter . . .



How to Buy and Use Minicomputers and Microcomputers, *by William Barden Jr, Howard W Sams and Co Inc, Indianapolis, 1976, 240 pages, 8½x11, paperback, $9.95.*

William Barden Jr has written an interesting new book entitled *How to Buy and Use Minicomputers and Microcomputers.* The book is designed with the new user or potential user in mind, as is reflected by the following excerpt from its preface:

> *It doesn't take a mathematical or electronics genius to learn how to use and program one of these computers. Starting with a basic system, a beginner can learn by writing two- or three-step programs and rapidly work up to larger and more complicated functions. The beginner may then add to his basic system as his hobby (and pocketbook) grows. A minimum system is now in the $200 range.*
>
> *The purpose here is to instruct the interested person in what computers are, how they perform their computing, and what tools are necessary to talk to all computers, especially the newer minicomputers and microcomputers. A detailed description of four low-priced minicomputers and many lower-priced microcomputers is included. Many examples of "real-world" connections to computers are given, as are short programs illustrating the programming of the computers both in the more rudimentary machine language and the BASIC language. Benchmark programs for every minicomputer or microcomputer discussed are provided for comparisons of one computer with another.*

Further, the book reflects an important point, which we can only emphasize over and over again: microcomputers, per se, are merely extensions of the concept of a minicomputer to a lower price range. As such, the book is about inexpensive general purpose computer systems, rather than exclusively concentrating upon the microcomputer as a currently fashionable and practical way of implementing the processors for such systems.

You'll find a chapter on the basics of computers, a chapter on the hardware of processors, a chapter on software, an excellent and comprehensive chapter on peripheral devices from the standard to the nonstandard, a chapter on how to select a system, a chapter on programming and applying a system, and two chapters profiling general purpose systems based on microcomputers and minicomputers. The book is finished with a set of 10 appendices and an index. We highly recommend this book as a background source of information for the new computer user who wants to get oriented in the field as quickly as possible. . . CH■

Electronic Projects for Musicians, *by Craig Anderton, Guitar Player Productions, Saratoga CA, 1975, $6.95.*

If brevity is the soul of wit, clarity and conciseness are the life's blood of a good technical handbook – especially when a neophyte's comprehension is at stake. That's what makes this text so satisfying. The beginner's understanding is not short-circuited by seemingly groundless technical lingo. Rather, the reader is led by a friendly hand through the wirey labyrinth of integrated circuits, resistors and capacitors. Within fifty pages, even a novice is well on the way to building his or her own preamps, metronomes, sound mixers, tone controls or any of fifteen other musical projects.

With Anderton's light readable style and Vesta Copestake's clear illustrations and schematics, Chapter one's introduction to electronics is quick and relatively painless. The musician may not learn everything, but he or she will pick up enough theory to take off the gloves and just about get to work.

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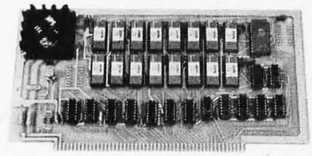
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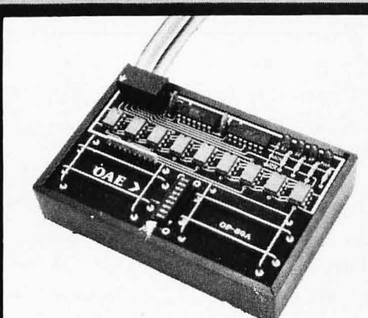
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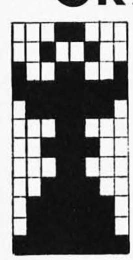
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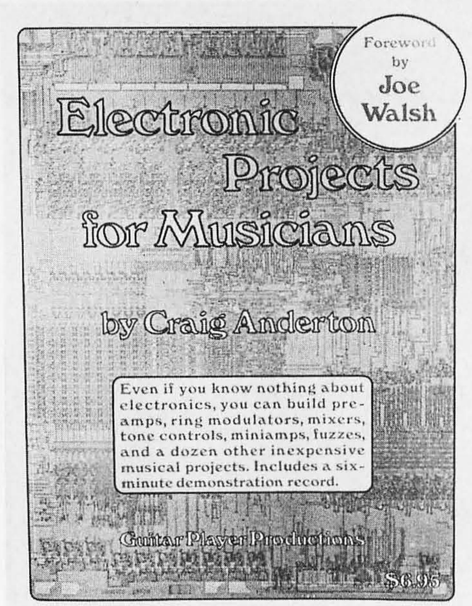
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prices. Included is a log of mail order suppliers, a representative price list of retail and wholesale components, and some warnings on detecting bad deals.

The author also assembles a decent set of tools for about sixty dollars, which should pay for itself within a few projects. Included are pointers on the care and feeding of tools as well as some safety tips: "Don't solder with shorts on if you're sitting down. Sometimes the rosin spits out and hits you on the leg."

Once the tools, parts, and basic theory are together, the next step is construction – perfboard assemblage, soldering, drilling templates and the like. With the clear instructions for basic workmanship digested, even the greenest are now ready to disappear into the basement for some hands-on experience.

Each of the projects uses one integrated circuit, runs on common battery voltages, and requires about the same level of technical competence. For each gadget, the author explains just what it does (a record comes with the book to show how each sounds), as well as how to build, substitute, or modify. Included for every project are schematics, parts lists, component layout diagrams, and a one-to-one scale positive of the board foil pattern.

The appendix gives approximate material costs for the projects (at December 1975 prices). The most expensive project, an eight-in-one-out mixer, is listed at $20 to $40. The rest range from under $5 to about $25. Not bad when you consider the manufactured costs; and, with Anderton's help, not all that difficult to build either. Even if you haven't the faintest interest in electronic music projects, the practical pointers on identification of parts and construction of electronics projects make this book an essential starting point for us novices.

Jim Travisano
Box 4
Marlboro VT 05344 ■

The Compleat Computer *by Dennie Van Tassel,* Science Research Associates, Chica*go, 216 pages, softbound, $5.95.*

RIDDLE: What do a medical center, the Senate Watergate Committee's investigative team and a Tibetan monastery have in common? ANSWER: a computer. Surprised? Thanks to Dennie Van Tassel's *The Compleat Computer*, such information about the increasing use of computers has lost much of its stiff scientific "byte" and been replaced with beneficial information that anyone can understand.

The Compleat Computer (1976), a carefully compiled collection of over 100 informative and often humorous articles by noncomputer specialists, seems to be the best publication so far to help expose people to the many diverse opinions about the computer. Author Van Tassel, user liaison in the computer center at UCSC and collector of computer miscellany, has filled his paperback book with a wide variety of selections from fiction, poetry, newspapers, cartoons and advertising as well as articles that concern the computer specialist. Such well-known noncomputer experts as Norman Cousins, Ray Bradbury and Issac Asimov are just a few of the writers whose articles appear in the book.

Some of the different areas covered include the story of a fully computerized poison control center in a children's hospital in Missouri, a computer which acted as a key "member" of the Senate Watergate investigative team by spewing out minute facts about any witness in a fraction of a second and a fictional account of how a Tibetan monastery might use a computer to compile a list of all the possible names of god.

In order to include as much material as possible, Van Tassel capsulized the longer articles and selected only the "tastiest tidbits" for publication. His extensive references following each article are helpful to the interested reader who wishes to pursue a topic in greater depth. After each well-

organized section of the book, a long list of questions and exercises is included to further aid the reader in exploring other various opinions about the use of computers.

The book is divided into nine sections starting with three introductory chapters which discuss the basics of computers. Articles appearing in this first section include "The Development of Automatic Computing," "Computer Games People Play" and "Technology, McDonald's Collide as Students Best Burger Bonanza," a humorous article describing how Cal Tech students used an IBM computer to print out 1.2 million entry blanks and win a McDonald's contest.

The seond portion of the book brings the reader up to date with chapters on "The Present and Potential," "Applications" and "Governmental Uses" of computers. In "Justice, the Constitution and Privacy," Sam Ervin Jr, Senator from North Carolina, raises some interesting questions concerning the computer's role in government surveillance and the individual's right to privacy. On a more humorous side, Art Buchwald's "The Curse" warns of the horrible consequences a computer metes out when a defiant citizen dares to fold, bend and mutilate his phone bill and send it (with payment) back to the company.

The book's final three chapters, "The Impact of Computers," "Controls or Maybe Lack of Controls" and "Your Future," explore the many significant effects the computer has upon our everyday lives and the potential it plays in our country's future. Articles in this section include "Computerized Dating or Matchmaking," "Computer Crime" and "Machines Hold Powers for Good and Evil."

Interspersed among the many informative articles are imaginative poems, computer generated illustrations and cartoons. Throughout the book the famous comic strip character Doonesbury and his friend Mark marvel at the many wonders of the computer. A newspaper ad for computer operators convinces them that they have found their true vocation in life. "Earn $7,000 . . . impress your friends . . . MEET GIRLS!"

In addition to all that humor, intrigue and important information to both the computer and noncomputer specialist, *The Compleat Computer* also offers a fictional romance about a computer named Max who almost breaks up a marriage. For $5.95 a copy, who could ask for more? Van Tassel has also written *Program Style, Design, Efficiency Debugging and Testing* (Prentice-Hall Inc).



Behind every successful computer . . . there stands a human being.

Linda Blocki
1706 Silver SE, Apt 27
Albuquerque NM 87106 ■

Continued from page 48

your particular interface carefully. What is even worse is that this procedure will probably destroy blanking during vertical and horizontal retrace. The easiest way out of the blanking problem is to gate the output of the added inverter with the various counters provided on the interface in such a way as to provide a black on white image only in the character field of the display. This will leave ugly black borders on the screen, but they are preferable to a lack of blanking.

The next problem involves generating subjective color timing pulses such as those shown in figure 3. This turns out to be a very easy problem to solve. A 60 Hertz nonsymmetric clock is certainly available at the interface since it is needed to generate the vertical sync pulse for the television. A 7492 TTL IC configured as a divide by twelve counter and a two input NOR gate are all that is required to generate the color timing pulses in figure 3 from the 60 Hertz clock. We want the first flip flop, the A stage, in the counter to trigger every time a vertical sync pulse goes out, but we do not care whether it triggers just before or just after the sync pulse. Thus, the fact that the counter is triggered by a falling edge is likely to be just interesting trivia.

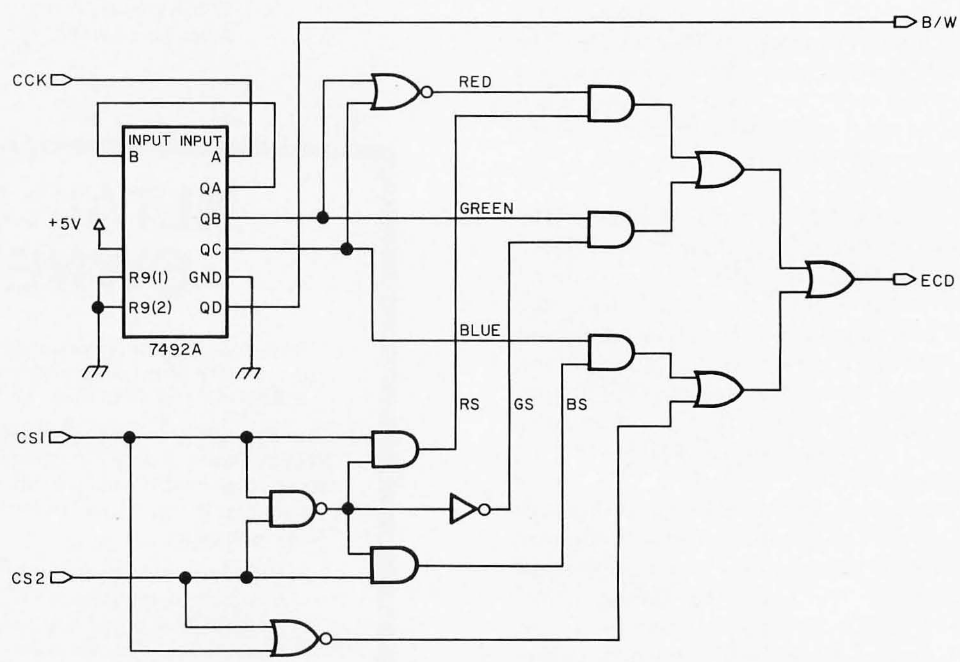
Another problem is providing for the storage and readout of the color information. The simplest and most versatile approach is to provide separate color information for each character. If we provide for four character colors: black, red, green and blue, we need to provide two extra bits of storage at each character address. If you have a video interface such as TVT II which only implements a 64 character subset of ASCII, both color and character information can be stored in a single 8 bit byte. Since virtually all of the small computers for personal use are byte oriented, this configuration is particularly appealing. You may wish to use it even if your video interface is capable of generating the full ASCII character set.

A suggested but arbitrarily chosen code for the two color select bits is also provided in figure 3 along with explanations for

REFERENCES

James F Butterfield, inventor of a subjective color translator, assesses the effects in his article in:
Journal of the Society of Motion Picture and Television Engineers, Volume 17, page 1025, 1968.

Other articles have appeared in:
Broadcasting, April 11 1967.
Wall Street Journal, July 24 1967.
Electronic Design, September 13 1967, page 38.
Popular Electronics, October 1968.



B/W	ECD	REQUIRED ACTION
0	0	DO NOT DISPLAY THE CHARACTER; INSTEAD DISPLAY BLACK
0	1	DO NOT DISPLAY THE CHARACTER; INSTEAD DISPLAY BLACK
1	0	DO NOT DISPLAY THE CHARACTER; INSTEAD DISPLAY WHITE
1	1	DISPLAY THE CHARACTER AS BLACK DOTS ON A WHITE SURROUND

Figure 4: The heart of a subjective color generator. CCK is the input from the 60 Hz nonsymmetric clock, CS1 and CS2 are the color select bits read in from memory. The two outputs, BW for black and white, and ECD for enable character display, are used to gate the output of the character generator to provide the table.

various abbreviations. The color select bits can be decoded with a 74155 TTL demultiplexer, but random logic is less expensive. The color select bits are to be read into and out of memory at the same time as the character bits so the same address lines and timing can be used for both.

Figure 4 is a logic diagram of the heart of a black and white to subjective color converter. Its inputs are the previously mentioned 60 Hertz nonsymmetric clock and the two color select bits which are read from memory. Its outputs are two signals which are to be used to gate the output of the character generator's shift register in such a way as to provide the results listed in the table in figure 4. Please note that figure 4 is drawn for pedagogic value rather than for package minimization.

Some Final Notes

In adding subjective color to your current video interface you will certainly want to include an override switch since you will likely find the black on white display and the subjective color flicker to be somewhat distracting in noncolor applications.

For best results the video display on which subjective color is implemented should be placed where there is moderate ambient light, preferably from incandescent lamps. Since the phosphors on most black and white television sets produce a white of high color temperature, you will find that an overall filtration of the CRT face with a large acetate warming filter is useful in producing the best reds.

You can produce subjective colors on a color set, but the technique works best on a black and white set. This is due to the black and white set's superior contrast and resolution.

The best time to think about implementing subjective color is *before* the design of a video interface. Perhaps this article will be the catalyst for some new products.

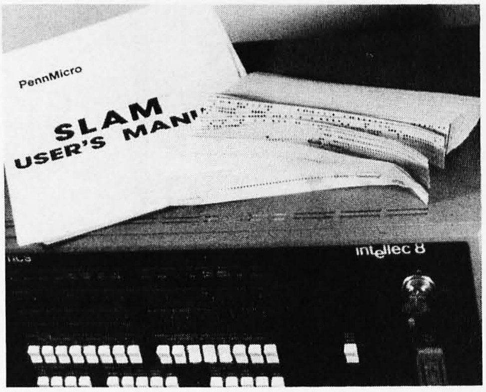
Will subjective color knock Cromemco and Intelligent Systems on their respective ears? Hardly. Its advantages are obvious but its performance is modest. Subjective color should be viewed as an interesting and useful method of displaying occasional color information on a black and white video terminal.■

How Well Will It Work?

This is an idea article. The details of implementing it in any particular system must be worked out by the experimenter. We'd like to see some feedback from readers who actually implement this experiment . . . CH

What's New?

SLAM: A Software New Product for Professionals



A company called PennMicro, POB 5073, Lancaster PA 17604, has announced the availability of SLAM, a compact improved operating system designed to operate on Intel's Intellec 8/MOD 80 and MDS Microcomputer Systems. According to PennMicro, SLAM makes these microcomputers far more powerful and easier to program by providing a text editor and high level language interpreter in a package occupying less than 3200 bytes of memory. The aim of the package is to give the user a facility to create a program using the text editor, then run it immediately using only the microcomputer and a Teletype. This eliminates paper tape operations completely without the cost of a diskette. Since SLAM uses a high level language similar to BASIC, programming is faster and easier than assembly language usually used with microcomputers. SLAM (Symbolic Language Adapted for Microcomputers) sounds a bit like Tiny BASIC: It uses 16 bit signed numbers for convenience, has IO and bit masking operations, has a variety of conditional and subroutine commands, and is totally symbolic in nature . . . the user need not assign registers or memory addresses. An optional SLAM feature permits program development while the microcomputer is operating other real time systems.

SLAM is loaded and entered using the Intel System Monitor. It is supplied on paper tape, ready to load without modification. A complete instruction manual is supplied. SLAM is available directly from PennMicro for $99; delivery is quoted as stock to two weeks. Customers should specify whether Intellec or MDS version is desired and whether provision for interrupts is desired. For users of these Intel Systems, SLAM sounds like an excellent way to get instant high level language capability.■

Attention Music Lovers

Chateau Engineering Co, POB 11, Arlington VA 22210, manufactures a system called SCORTOS, which is a completely automated music score editing and performance system built from an Altair 8800, an ADM-III Video Display Terminal, a cassette or floppy disk mass storage device, and their special hardware product, the "Keyboard Interface Controller." This system is designed to interface mechanically with existing keyboard instruments, so that scores edited in the computer can be played in real time. As commented in the brochure, "The computer converts musical symbols to musical events much the same as does a musician; in fact the SCORTOS system can be thought of as an organist with sixteen hands since it is capable of performing sixteen separate parts simultaneously." The key item, the Keyboard Interface Controller, operates by switching mechanical relays and is completely electrically isolated from the instrument it is controlling. This facilitates the connection of instruments to SCORTOS, since electrical characteristics ranging from none (as in a piano) to extensive (as in electronic organ or Moog synthesizer) need not be a consideration. Each KIC controls two octaves of keyboard, or 24 keys, but the system can handle up to 11 KIC units. The response time of the mechanical relays is 10 ms, and up to 255 keys can be controlled with up to 22 KIC units. In a one drive floppy system, 80,000 musical events can be stored on line for up to 16 channels. The software described in the brochure is a music description language edited with a specially configured ASCII keyboard.

The price? A cassette based system with one KIC output unit starts at $8000. A floppy disk based system can be purchased with one KIC output unit starting at $10,000.■



Here is a Neat Little 8 K 6800 System

Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110, (714) 276-8911, has announced a complete, self contained 6800 system for $1186 called the Expanded-68. Designed primarily for system prototype development use, the Expanded-68 comes complete with 8 K of memory, power supply, 16 digit keyboard, hexadecimal LED display, expansion cabinet, 36 pin edge connector, and MIKBUG as an operating system. Also available for direct interfacing are: dual floppy disk drive, IMP-1 printer, 132 column printer, TV interface, and full ASCII keyboard. However, even if you're not a systems engineer designing new products, you may find this 6800 in its attractive desk top package will prove to be an interesting personal computer option.■

Software New Product

Are there bunches of PDP-8 users buried in the woodwork? Of course there are, since Digital Equipment Corp's PDP-8 started the growth of the small computer field, and is probably the widest selling minicomputer prior to the microcomputer revolution. There is even the IM6100 copy of the PDP-8 which is a CMOS microcomputer which represents a dedicated applications route to a PDP-8-like system.

Recognizing this presence of the PDP-8 (which is still a very widely sold product in DEC's stable), a firm called EDUCOMP, located at 196 Trumbull St, Hartford CT 06103, has been active in the independent software market for PDP-8 compatible products, with the star attraction being a PDP-8 operating

system called ETOS. This software has just been cycled through to version 4B, which was described in a recent press release. ETOS version 4B provides timesharing, real time tasks, and batch processing simultaneously. Real time programs supported under this release typically include device handlers for time dependent tasks such as process control and data acquisition. With ETOS 4B real time tasks can be serviced while background users continue to operate undisturbed under timesharing.

The operating system includes a lot of useful "big computer" OS features not normally associated with minicomputers. For those readers with PDP-8 computers, multiple disk drives, multiple terminals and professional level requirements, this $4,900 operating system package may well be worth your investment. For further details, contact EDUCOMP Corp.■

BYTE's Bugs

APL COMMENTARY

I was extremely pleased to see an article on APL in your magazine. There were a few errors, however, possibly because of the stated difficulty of achieving "Selectric" quality printing fonts.

Of particular interest was the author's inconsistent use of the non-APL symbol "ε." No such symbol exists to my knowledge. He uses it for *two* operations: execute (⍎) *and* membership (∈).

A minor typo: in APL, 2×3+4×5 is 46_{10}, not $56_{?}$.

Although explained well, the negative sign (¯) was incorrectly used in the explanation of take and drop (↑, ↓). The correct symbols are ¯N↑A and ¯N↓A. The subtract sign (−) was used erroneously (negation).

If J were a scalar, X/J would *not* yield the same result as !J. What was probably omitted was an iota; ie: X/ιJ.

The T-bar symbol is new to me. It is not used in the 3.0 release of the IBM program product nor in the APL plus system nor Honeywell's file management version. I suspect format (⍕) was meant.

Despite my nit-picking, my utmost encouragement to Mr Arnold in developing an APL interpreter.

Carmen J D'Agostino■

Where Is It?

John G Madry Jr, MD, Melbourne FL 32901, calls our attention to our omission of the address for Executive Devices, which makes the pocket data terminals described on page 99, November 1976 BYTE. The firm is located at 740 S Logan, Fresno CA 93727; phone (209) 255-6977.■

Further Notes on Bar Codes

The reactions to bar code as a means of printing programs have been quite encouraging. We've received a flood of letters with numerous comments ranging from "great" to "scurrilous" [*hard to believe*], from no technical content to multiple page tomes of opinionated technical proposal.

We had planned to put in a little bar code contest this month, but a number of circumstances at the production end added together in phase to prevent the copy from reaching the magazine for February. The production of bar codes in this form is still a very experimental art... The tricks which Walter Banks had to pull, together with the usual programming glitches and circumstances totally unrelated to bar codes or programming made themselves evident when February's bar code information was prepared.

The first output came our way well in advance of the publication deadline. The mental model at that point was "everything's just fine." Then, along about two weeks before press time, yours truly decided that it might be a good idea to try decoding the copy. A test decode of the copy found a bit of a discrepancy. It turns out that there was a minor bug in the conversion software: 9 bits instead of 8 bits per byte. (The program was run on a machine with a 36 bit word... hmmm sounds suspicious).

So Walter went back to work on ironing out the bug — only to find that after fixing the program a crucial step in the process of bootstrapping the minicomputer in the Photon phototypesetter decided to die: The stepper motor in the paper tape reader of the machine burned out. In a feat of real time hardware redesign, on the weekend of December 11-12, Walter and associates discarded (logically) the paper tape reader and added another direct hardwired link to the Honeywell computer which enabled them to bootstrap directly. The actual data for the bar codes had always been sent directly over a communications link, which is a good thing, since for just one 6.75 by 3 inch (17.1 by 7.6 cm) segment of bar code copy the machine requires over 70,000 commands.

Finally, to cap off the whole process, three days before the deadline, Walter sent the package containing the bar code samples for this issue, and they were promptly lost by the air express company which was used as a courier. As is usual in magazine practice, we prepared this alternative set of copy to go with the magazine — in case at the last minute the missing bars were to arrive like cavalry and save the day.■

TTL Loading Considerations

Greg Tomalesky
Design Engineer
GT Electronics
164 Preston Rd
Parsippany NJ 07054

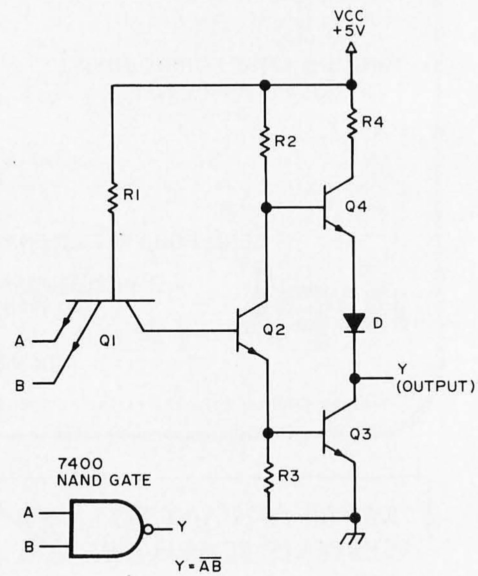


Figure 1: Schematic Diagram and symbolic representation of a simple 7400 NAND gate. The inputs are A and B and the output is Y.

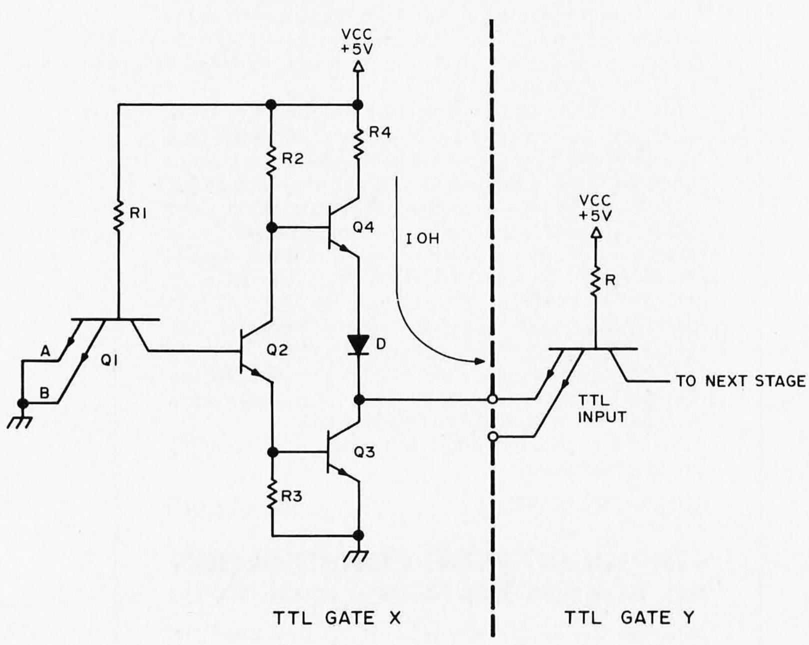


Figure 2a: Schematic Diagram of a basic TTL gate showing the direction of IOH when the output is high, VOH.

If you have ever studied a microcomputer's schematic diagram, chances are you have seen gates, flip flops, memories, etc, connected together to perform certain tasks essential to the operation of the computer. Upon closer examination you should notice that various logic families are mixed, such as 74XX, 74LXX, 74LSXX and perhaps even CMOS. However, you may not have noticed that there is a limit to the number of gates that may be interconnected. The purpose of this article is to show how these limitations are arrived at by circuit designers and what you should watch out for in your own circuit design.

Let's take a close look at what goes on inside a typical gate and apply this knowledge to our circuit design. Figure 1 is a schematic diagram of a standard TTL NAND gate model 7400. The input of this gate is a multiemitter transistor, Q1. The base of Q1 is tied to VCC, +5 V, through R1. This arrangement turns Q1 on and allows current to flow from emitter to collector (see Bibliography, reference 1, for further discussion of this circuit). When both emitters are at a logical 1 voltage, 2.4 V ≤ VIH ≤ VCC, this current flows through Q1 and turns Q2 on. With Q2 on, Q3 is also on, and it conducts from collector to ground. This causes a logical 0 voltage, (0 V ≤ VOL ≤ 0.4 V, to appear at the output.

In the case where both emitters are grounded, no current flows to Q2 and it remains in the off state. With Q2 off, Q3 is also off. Q4 is now on and a logical 1 voltage appears at the output. Table 1 is a truth table summarizing input and output for the circuit.

The current for the input transistor Q1 is set by varying R1. A large value for R1

y = AB (NAND)

B \ A	0	1
0	1	1
1	1	0

Table 1: Truth Table for the NAND circuit shown in figure 1. The inputs are A and B and the output is Y.

results in a lower input current, IIH and IIL, for the various TTL families.

On the output side, the currents IOH and IOL are determined by Q3, Q4, R2 and R4. For a logic 1 voltage, this current is flowing out of the output and is governed by R4. In the data books this current is given a minus sign to indicate current flow out of a terminal. Low values of R4 allow higher output currents for single transistor output stages. In some cases, such as the 74S series, a Darlington transistor pair is used to boost the output current beyond that obtainable with a single transistor.

Figures 3a and 3b illustrate the direction of current flow for VOH and VOL respectively. In table 2 the output currents are given for the various TTL families. Circuit designers use the values of IIH, IIL, IOH and IOL to calculate the fanout. Fanout is a measure of the number of inputs which may safely be connected to one output.

The fanout between two logic families may be calculated in one of two ways. Table 3 gives the fanout based on IOH and IIH. The results of the division (IOH/IIH) are given as absolute values in table 3. Absolute values are used because negative fanout has no practical meaning. Table 4 gives the fanout values calculated from IOL and IIL. Again the absolute value is taken. To find the number of inputs that may be driven from one output, one simply locates the driving output family across the top of the chart and proceeds down that column to the row corresponding to the driven input. This procedure should be followed for both charts since the fanout values will be different depending on the mode of calculation. As an example, using table 3, we want to know how many 74L series inputs may be driven by one 74S series output. By following the above directions, we see that this value is 100 inputs. Using table 4, we notice the value is more than with table 3. In this case the limiting value is the smaller of the two. Since the figures are based on manu-

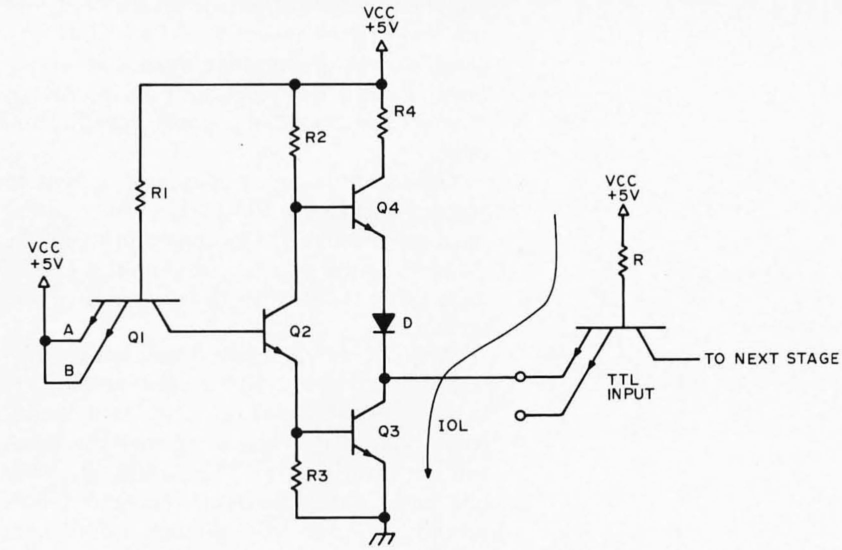


Figure 2b: Schematic Diagram of a basic TTL gate showing the direction of IOL when the output is low, VOL.

	74	74L	74H	74S	74LS
IOL (mA)	16	2	20	20	4
IOH (μA)	−400	−200	−500	−1000	−400

Table 2: High and low output currents from several different TTL devices.

Driven Input	Driving Output: 74	74L	74H	74S	74LS
74	10	5	12	25	10
74L	40	20	50	100	40
74H	8	4	10	20	8
74S	8	4	10	20	8
74LS	20	10	25	50	20

Table 3: Fanout Chart used to compute the number of devices any particular TTL device can power. The fanout is calculated by dividing the output current by the input current. In this case the highest input and output values were used.

Driven Input	Driving Output: 74	74L	74H	74S	74LS
74	10	1	12	12	2
74L	88	11	111	111	22
74H	8	1	10	10	2
74S	8	1	10	10	2
74LS	44	5	55	55	11

Table 4: Fanout Chart calculated the same way as table 3 except that the lowest values of input and output current were used in the calculations.

facturers' specifications, they are valid over the temperature range $0C \leqslant Ta \leqslant 70 C$ for a given part and represent worst case conditions. Fanout decreases with an increase in temperature above the upper specification limit.

Gate outputs must also sink current to ground during the VOL state. This current must go through Q3 as shown in figure 2a. As is often the case, a gate output is able to drive more inputs high than it is able to sink at VOL.

When doing your own circuit design, plan out your connections to avoid exceeding the fanout specifications as calculated above. Remember also, when using multiple input gates as inverters, ie: 7420, 7400, etc, only one input should be used. The other inputs should be tied to VCC through a 1000 ohm resistor. It is also good practice never to tie unused inputs to used inputs because of the increased current drain. As an example, each input of a 7400 NAND gate requires 40 μA at IIH. If both inputs are tied together to act as an inverter, the resultant input current would be 80 μA or the sum of the two input currents. On the other hand, if one input is used while the other is tied to VCC, the current of the active input is 40 μA. Also, do not tie two or more outputs together. If all the outputs are high it's okay, but as soon as one goes low it will try to bring the others low also. This will result in faulty performance or at worst a damaged gate.

In addition to the charts and tables described here, be sure to consult any pertinent data books for further information as to specifications, pin connections, etc. If you are just getting started in digital circuit design, it may be helpful to look over published schematics to get some ideas and also to compare calculated fanout data.

Digital design can be both rewarding and frustrating; however, by paying close attention to the recommended design practices, you will insure yourself against frustration and produce better circuit designs.■

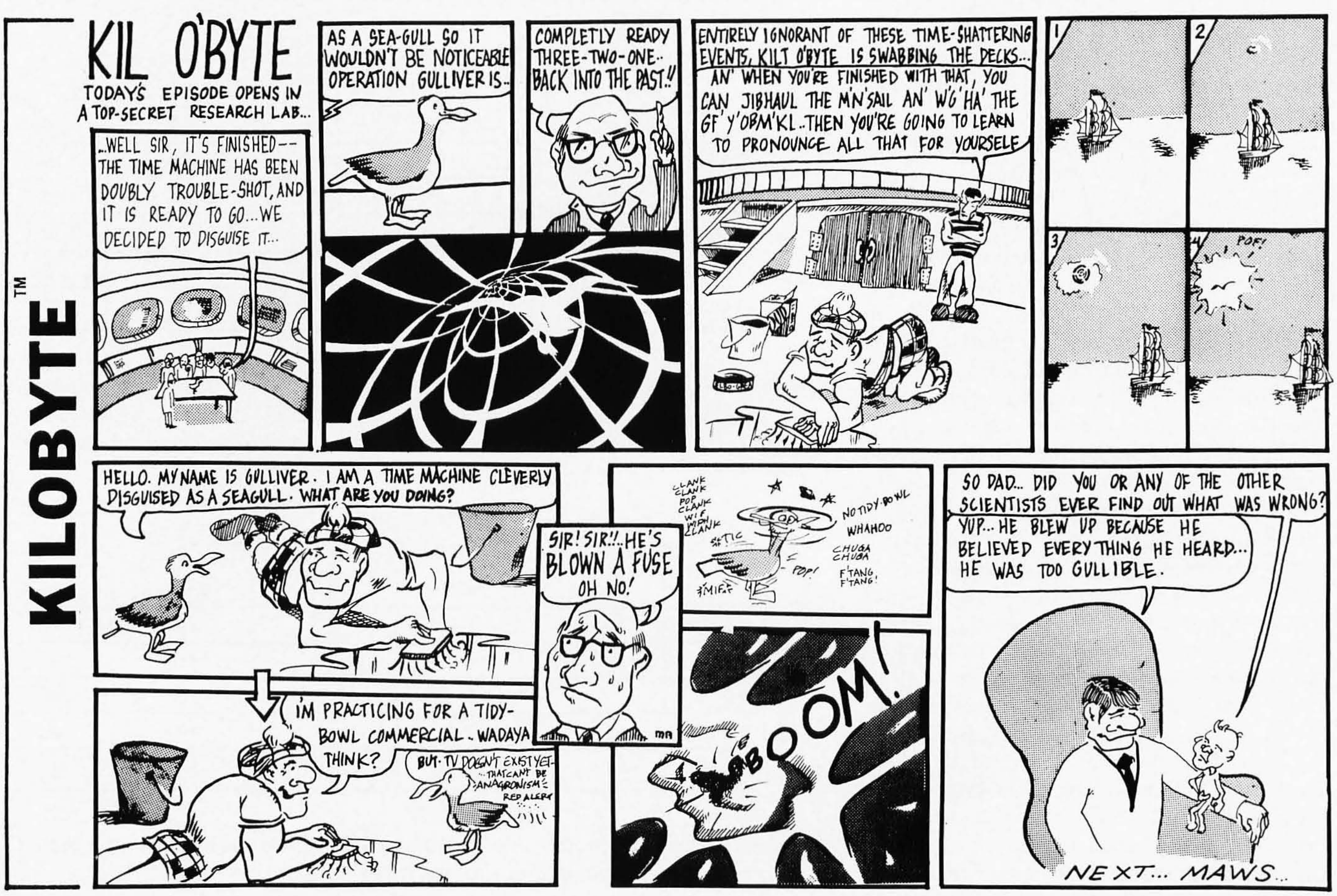
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Ted Nelson. This book is devoted to the premise that everybody should understand computers. In a blithe manner the author covers interactive systems, terminals, computer languages, data structures, binary patterns, computer architecture, mini-computers, big computers, microprocessors, simulation, military uses of computers, computer companies, and much, much more. Whole earth catalog style and size. A doozy! 127 pp. $7.00 [8P]

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Joseph Weizenbaum. In this major new book, a distinguished computer scientist sounds the warning against the dangerous tendency to view computers and humans as merely two different kinds of "thinking machines." Weizenbaum explains exactly how the computer works and how it is being wrongly substituted for human choices. 300 pp. $9.95 [8R]

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Ruth Leavitt, ed. Presents personal statements of 35 internationally-known computer artists coupled with over 160 plates in full color and black & white. Covers video art, optical phenomena, mathematical structures, sculpture, weaving, and more. 132 pp. $4.95 [6D] Cloth cover $10.95 [6E]

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Ted Sage. This text is designed to be used in a one-semester course in computer programming. It teaches BASIC in the context of the traditional high school mathematics curriculum. There are 40 carefully graded problems dealing with many of the more familiar topics of algebra and geometry. Probably the most widely adopted computer text. 244 pp. $5.95 [8J]

A Simplified Guide to Fortran Programming

Daniel McCracken. A thorough first text in Fortran. Covers all basic statements and quickly gets into case studies ranging from simple (printing columns) to challenging (craps games simulation). 278 pp. $8.75 [7F]

Understanding Solid State Electronics

An excellent tutorial introduction to transistor and diode circuitry. Used at the TI Learning Center, this book was written for the person who needs to understand electronics but can't devote years to the study. 242 pp. $2.95 [9A]

Microprocessors

A collection of articles from *Electronics* magazine. The book is in three parts: device technology; designing with microprocessors; and applications. 160 pp. 1975 $13.50 [9J]

Microprocessors: Technology, Architecture and Applications

Daniel R. McGlynn. This introduction to the microprocessor defines and describes the related computer structures and electronic semi-conductor processes. Treats both hardware and software, giving an overview of commercially available microprocessors, and helps the user to determine the best one for him/her. 240 pp. $12.00 [7C]

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BYTE's Bits

A Computer Oriented Radio Talk Show

Richard Gardner has made some connections in the radio media resulting in a new radio "talk" show for computer people which began 11 am-12:30 pm on January 22 1977 over radio station WBUR in Boston. Guests lined up for the early shows include:

> Calvin Mooers, Rockford Research, discussing patent and copyright laws as applied to computer programs, documentation, proprietary software and software security.
>
> A representative of ECD Corporation, Cambridge MA, manufacturers of a most interesting and complete computer system with high resolution graphics.
>
> Bill Rosenfeld, MIT Lincoln Labs, a researcher working on topics of speech compression and speech synthesis.
>
> John Carroll, Dynamic Measurement Corporation, who designs power supplies and other electronic equipment professionally, discussing ideas for broadcasting programs and data over the air and how individual users might record this information for personal use.
>
> Arra Avakian, owner of a KIM-1, discussing some of the finer points of using this 6502 based system.
>
> Carl Mikkelson, Intermetrics Inc, talking about the development of the PLM6800 compiler, a language translator for cross compilations using large machines.
>
> Quincy Bent, Shriver Foundation, describing how he has been using a microcomputer kit to build a video tape editing system – in spite of his total lack of familiarity with computers prior to the project.
>
> Karen Brothers and Louise Silver, programming consultants, who have a PDP-8 based home computer system, discussing how they do recipe nutrient analysis so that given a recipe, its nutritional value can be computed. Their data base on nutrition includes everything from reindeer milk to muskrat's tail.

Initial versions of the show have been done using a local radio talk show format over WBUR, the Boston University radio station. Richard reports that he has been discussing the prospect of syndicating the show through the PBS network or commercial radio as an educational and informative program for people who are interested in small computers. We'll have further reports as

time progresses. Richard can be reached by phone at (617) 354-1216 (leave a message in response to his unusual phone reply tape if he's not there) or write him at Box 134, Harvard Sq, Cambridge MA 02138.■

Publicity

Our Canadian readers will be interested to know that there is now a bona-fide computer store in operation in Canada. The store will carry a very broad range of products of interest to all users, from hobbyists to small scale business systems.

The First Canadian Computer Store Ltd is located at 44 Elington Av, Toronto, Ontario M4R 1A1, (416) 482-8080.■

The Southernmost Computer Store

Sunny Computer Stores Inc has moved to a permanent location in the University Shopping Center across from the University of Miami. They offer a full line of computers, components, books, magazines and a complete service center for all products carried.■

Attention Educators

The 1977 Winter Meeting of the Association for the Development of Computer-Based Instructional Systems (ADCIS) will be held in Newark DE, February 22 thru 24 1977. For further information, contact the conference host, Fred Hofstetter, Department of Music, University of Delaware, Newark DE 19711, (302) 738-2497.■

Computer Warehouse Store Opening

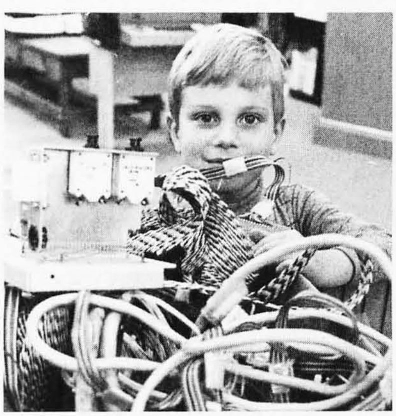
On Thursday, November 18, the Computer Warehouse store in Boston held its grand opening celebration. Here is a cross section of pictures supplied by Vic Farmer of the store, showing some of the action.



The maker of the potted palm is unknown, but computer-watchers will identify a rare Memorex MRX-40 (an IBM/360 Model 40 look-alike internally) under the palm, with an early DEC PDP-8 at the right. Since the Computer Warehouse store combines all the delights of a surplus house (it's the back side of American Used Computer) and a regular computer store, it is definitely a "must stop" on any computer hacker's tour of the Northeast.



The official "crowd scene" shot taken with a wide angle camera.



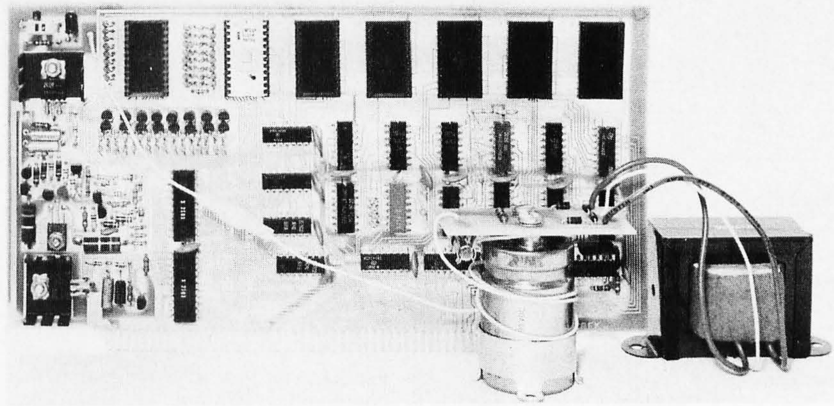


Two candid shots of budding hackers at work. From the looks of things, one is a hardware person and the other a software person.



One of the door prizes being shown to the door by its new owners.

What's New?



Take a Look, All Ye Timesharing Freaks, Microcomputer Users without Terminals

A company called the Computer Conversion Corp, located at 1961 Old Middlefield Way, Mountain View CA 94043, has just introduced this new terminal unit, priced as low as $595 for just one of the 40 character by 24 line models, Conversor 4000. The Conversor 8000 is an 80 character by 24 line model priced at $695 for just one. The purchaser has to supply his or her own monitor or converted television to accept the video output of this compact keyboard unit, and the computer interface of the device is RS-232 with switch selectable 110 or 300 baud data rate. To get a timesharing terminal, the unit requires addition of the accoustic coupler option for $110. An audio "beeper" option is also available for $30. This is a completely assembled unit, available with delivery from 30 to 60 days according to the press release. For further details contact the manufacturer of this fine unit.■



PRAMMER?

XYBEK, a new firm with one product at present, makes the "PRAMMER," an EROM programmer with programmable memory buffer and control EROM for the Altair 8800, IMSAI 8080 and other Altair bus compatible computers. This 2 K memory board contains 256 bytes of programmable memory and space for 1792 bytes of 1702A EROM. One of the 1702A sockets doubles as the 1702A programming socket. The PRAMMER is not an IO device, but occupies any 2 K slice of system memory. This kit is complete with its own 80 V power supply, features onboard timing independent of the processor clocks and contains its own microprogram for read and write control. No oneshots are used for timing. The 256 bytes of programmable memory may be used for a stack, for buffers, save areas, etc, eliminating the need for use of main memory already dedicated to other application programs. Complete standalone software for programming and copying 1702A EROMs is supplied with the PRAMMER kit in a single preprogrammed 1702A. Also included are the complete listings for PRAMSYS, an 11 function development system designed to reside in the 1792 bytes of EROM in the fully populated board and to interface with a Teletype compatible terminal. Also available is a 3 foot extension kit for bringing any of the 1702A sockets to a zero insertion force socket outside your system's cabinet. The introductory price for the PRAMMER kit is $189 and the extension kit is $15. Address inquiries to XYBEK, POB 1631, Cupertino CA 95014.■

Attention Commercial and Industrial 6502 Users:

A PDP-11 Cross Assembler is Now Available

COMPAS has developed a PDP-11 based cross assembler for the MOS Technology family of microcomputers. The system is called the MINmic 1165 Cross Assembler and is written entirely in MACRO 11 (assembler language) and runs under the RT 11 operating system. It requires less than 5 K words for a minimal system and can be easily expanded to assemble larger programs if desired.

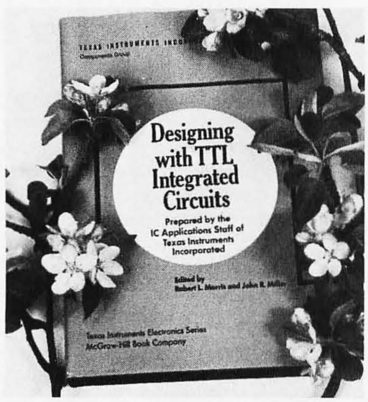
COMPAS is the firm which developed and supported cross assembly software for MOS Technology's 6502 marketing programs. The MINmic 1165 Cross Assembler is very similar to the FORTRAN based cross assemblers developed by COMPAS and offered nationally by MOS Technology. The system provides listing and memory files which conform to the standards established by MOS Technology for its products.

The MINmic 1165 Cross Assembler is priced at $900. The price includes a year's support. Source code is distributed on disk along with a test deck which verifies correct installation of the software. Further information is available from Mike Corder at (515) 232-8181.■

A BIT More

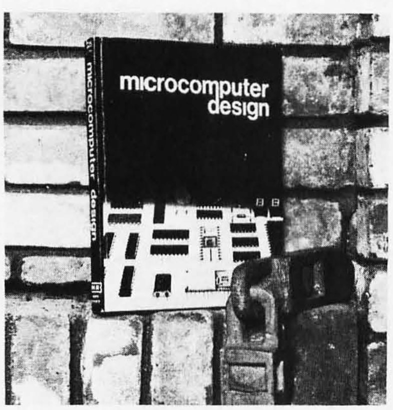
When you build a project, you need information. All you find in the advertisements for parts are mysterious numbers identifying the little beasties . . . hardly the sort of information which can be used to design a custom logic circuit. You can find out about many of the numbers by using the information found in these books. No laboratory bench is complete without an accompanying library shelf filled with references.





Order these absolutely essential references from Texas Instruments today:

___The TTL Data Book for Design Engineers, $4.95, new second edition.
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___The Power Semiconductor Handbook for Design Engineers, $3.95.
___Understanding Solid State Electronics, $2.95.
___The Optoelectronics Data Book for Design Engineers, $2.95.
___Designing with TTL Integrated Circuits, edited by Robert L Morris and John R Miller, published by McGraw-Hill, $24.



___**The TTL Cookbook** by Don Lancaster, published by Howard W Sams, Indianapolis. Start your quest for data here with Don's tutorial explanations of what makes a TTL logic design tick. 335 pages, $8.95.

___**Microcomputer Design** by Donald P Martin. Edited and published by Kerry S Berland, Martin Research. Purchase your copy of the definitive source for circuitry and hardware design information on the 8008 and 8080 computers today. Even Intel, the originator of the microprocessor revolution, is hard put to compete with the wealth of information found in Martin Research's new second edition of **Microcomputer Design.** This is the book which was originally published as an expensive (but quite practical) engineering report in loose leaf form, at about the time the microprocessor technology was first catching on in the form of the 8008. This 388 page second edition of the manual is loaded with detailed information on how to build and use computers based on the 8008 and 8080. $25.

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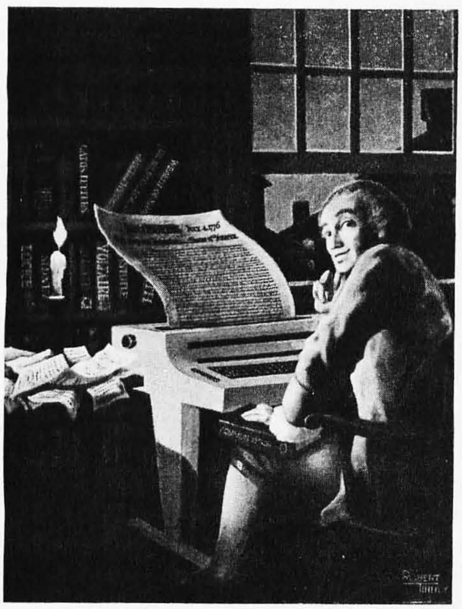
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It's Almost Too Late . . .

. . . to snap up bicentennial memorabilia before you have to hunt through the nostalgia shops and pay 100 times the original price—if you're lucky enough to find a bargain—for an item as anachronistic and otherwise remarkable as Robert Tinney's Computing 1776 picture.

A same-size (16 by 20 inches, 41 by 51 cm) reproduction of Tinney's original oil painting, this poster makes an off-beat gift.

Don't wait for the nostalgia shops to get the last of these posters; get yours now for only $2.95. (Do you know what your old Amazing Science Fiction magazines and Superman comics that Mom threw out are worth now?)



COMPUTER



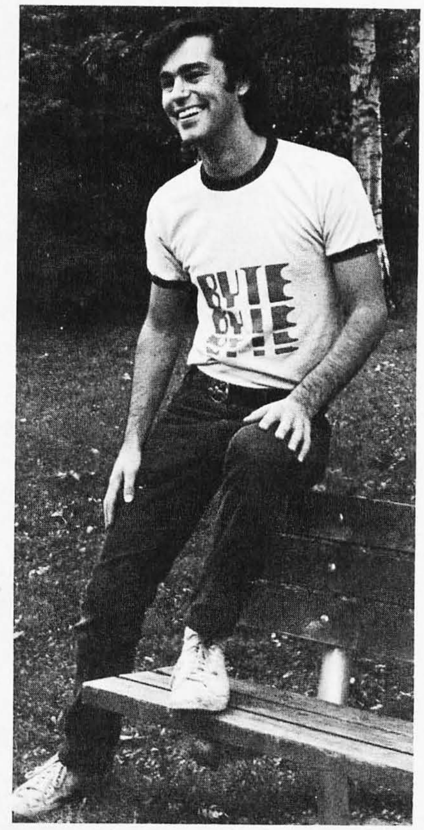
Have you ever wondered where to go for a basic starting point in your quest for information about computer applications and uses? Ted Nelson's book, *Computer Lib/Dream Machines*, is the place for you to begin.

Computer Lib/Dream Machines is for the layman — the person who is intelligent and inquisitive about computers. It is written and self published by a philosopher who is also a self confessed computer fan and an excellent teacher of basic concepts. (For those who have not yet heard, ivory towers are constructed out of real and substantial white bricks.)

Computer Lib/Dream Machines is must reading for the beginner, and is also a refreshing self examination for the old hand at programming and systems work.

BYTE T-shirts

Available in blue heather with blue trim and red letters, or in white with blue trim and red letters. Only $5, including postage and handling.



Please send me:

______copies of **Computer Lib** @ $7

50 cents postage per copy ________

Total________________

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Add Some BARC to Your 8080

Listing 1: The BARC Utility Routines. This listing contains the absolute octal code of the BARC routines. The notation <*> is used to indicate the absolute page address of the routines, which are loaded on a page boundary. When (for example) loading the routines at location 010/000, substitute the page address of 010 for the <*> every time it is seen in the listing. The code is in octal, for an 8080 computer. Refer to the "legend" box for explanations of some of the mnemonics in the commentary of this listing.

```
 Split
 Octal
Address   Octal Code     Label   Op     Operand    Commentary

<*> 000   353            SASNT   XCHG              USRRET=PLAD to DRDE; UDRDE to DRHL;
<*> 001   343                    XTHL              UDRDE to TOS; FRRET to DRHL;
<*> 002   305                    PUSH   B          UDRBC to TOS;
<*> 003   365                    PUSH   PSW        UDRPSW&A to TOS;
<*> 004   353                    XCHG              USRRET=PLAD to DRHL; FRRET to DRDE;
<*> 005   303 021 <*>            JMP    FRNTD      Go load only one field addr
                                                      and length parameter;
<*> 010   353            DASNT   XCHG              USRRET=PLAD to DRDE; UDRDE to DRHL;
<*> 011   343                    XTHL              UDRDE to TOS; FRRET to DRHL;
<*> 012   305                    PUSH   B          UDRBC to TOS;
<*> 013   365                    PUSH   PSW        UDRPSW&A to TOS;
<*> 014   353                    XCHG              USRRET=PLAD to DRHL; FRRET to DRDE;
<*> 015   116                    MOV    C,M        FIELD1 addr LOB to SRC;
<*> 016   043                    INX    H          Incr USRRET=PLAD (+1 DASNT);
<*> 017   106                    MOV    B,M        FIELD1 addr HOB to SRB;
<*> 020   043                    INX    H          Incr USRRET=PLAD (+2 DASNT);
<*> 021   325            FRNTD   PUSH   D          FRRET to TOS;
<*> 022   136                    MOV    E,M        FIELD/FIELD2 addr LOB to SRE;
<*> 023   043                    INX    H          Incr USRRET=PLAD (+3 DASNT; +1 SASNT);
<*> 024   126                    MOV    D,M        FIELD/FIELD2 addr HOB to SRD;
<*> 025   043                    INX    H          Incr USRRET=PLAD (+4 DASNT; +2 SASNT);
<*> 026   176                    MOV    A,M        Length/Size param to SRA;
<*> 027   043                    INX    H          Incr USRRET=PLAD (+5 DASNT; +3 SASNT);
<*> 030   343                    XTHL              True USRRET to TOS; FRRET to DRHL;
<*> 031   345                    PUSH   H          FRRET to TOS;
<*> 032   147                    MOV    H,A        Length/Size param to SRH;
<*> 033   311                    RET               Return to calling function routine;
<*> 034   343            DASXR   XTHL              UDRHL to TOS; FRRET=FRCOMMAND
                                                      address to TOS;
<*> 035   042 051 <*>            SHLD   DASFC+1    Store FRCOMMAND address in CALL;
<*> 040   341                    POP    H          TOS=UDRHL to DRHL clear return;
<*> 041   343                    XTHL              UDRHL to TOS; USRRET=PLAD to DRHL;
<*> 042   315 010 <*>            CALL   DASNT      Call DASNT to load parameters;
<*> 045   032            DASXL   LDAX   D          Indexed FIELD2 char to SRA;
<*> 046   157                    MOV    L,A        Move it to SRL;
<*> 047   012                    LDAX   B          Indexed FIELD1 char to SRA;
<*> 050   315 000 000    DASFC   CALL   Q'000000'  Call the execution commands;
<*> 053   002                    STAX   B          Store result in indexed FIELD1;
<*> 054   003                    INX    B          Incr FIELD1 address index;
<*> 055   023                    INX    D          Incr FIELD2 address index;
<*> 056   045                    DCR    H          Decrement length/size;
<*> 057   302 045 <*>            JNZ    DASXL      Loop until count is zero;
<*> 062   341            FRXIT   POP    H          True USRRET to DRHL;
<*> 063   301                    POP    B          UDRPSW&A to DRBC;
<*> 064   170                    MOV    A,B        USRA to SRA; PSW=FRPSW;
<*> 065   301            FRXT2   POP    B          TOS=UDRBC to DRBC;
<*> 066   321                    POP    D          TOS=UDRDE to DRDE;
<*> 067   343                    XTHL              True USRRET to TOS; TOS=UDRHL to DRHL;
<*> 070   311                    RET               Return to user; regs+user regs;
<*> 071   315 034 <*>    NCHR    CALL   DASXR      CALL DASXR execution control rtn
                                                      passing address of following;
<*> 074   245                    ANA    L          Logical AND SRL to SRA;
<*> 075   311                    RET               Return to DASXR;

<*> 076   315 034 <*>    OCHR    CALL   DASXR      See NCHR comment at address 071;
<*> 101   265                    ORA    L          Logical OR SRL to SRA;
<*> 102   311                    RET               Return to DASXR;

<*> 103   315 034 <*>    XCHR    CALL   DASXR      See NCHR comment at address 071;
<*> 106   255                    XRA    L          Logical XOR SRL to SRA;
<*> 107   311                    RET               Return to DASXR;

<*> 110   315 034 <*>    MVCHR   CALL   DASXR      See NCHR comment at address 071;
<*> 113   175                    MOV    A,L        Move SRL to SRA;
<*> 114   311                    RET               Return to DASXR;

<*> 115   315 034 <*>    SWCHR   CALL   DASXR      See NCHR comment at address 071;
<*> 120   022                    STAX   D          SRA to indexed FIELD2 char;
<*> 121   175                    MOV    A,L        Move SRL to SRA;
<*> 122   311                    RET               Return to DASXR;

<*> 123   315 034 <*>    CLCHR   CALL   DASXR      See NCHR comment at address 071;
<*> 126   275                    CMP    L          Compare SRL to SRA;
<*> 127   310                    RZ                Return to DASXR if equal;
<*> 130   077                    CMC               Else reverse inequality flag;
<*> 131   341                    POP    H          Clear return address by popping;
<*> 132   303 062 <*>            JMP    FRXIT      Bust out to function exit logic;
```


Charles Howerton
Digital Group Software Systems Inc
POB 1086
Arvada CO 80001

The programming convenience of a computer system is greatly enhanced by using software to extend the functions provided by the basic instruction set of the machine. Software to accomplish complicated functions like moving character strings or doing data conversions help the user to program manipulations of data in an application situation. This article is written to describe and give the code for a set of utility routines for the 8080 which can be used to advantage on any system employing this chip. This set of BARC utility routines is designed to assist the 8080 programmer in developing programs which involve the manipulation and validation of characters and character strings. The acronym "BARC" stands for BAsic Resource Capability. Almost all programs require these functions to a greater or a lesser extent if they accept input or generate output in any format other than absolute machine codes.

In all cases these routines are entered using an 8080 call instruction and in most cases the call instruction is immediately followed by a series of parameters which identify the field or fields to be acted upon, the length of the field or fields and in some cases an immediate value which is used in the requested function. The exceptions to this rule are the single character validation functions which require that the argument character be loaded into the accumulator prior to the call. In all cases (except the symbolic move) the user's register contents, with the exception of the program counter

WARNING

The BARC routines listed here will not work in read only memory or in write protected memory, since they modify program code as part of execution.

and flags, are returned with the same contents as they held prior to the call; the symbolic move routine returns the length moved in the accumulator with all other registers except the program counter and flags containing their original contents.

These routines all use the stack of the user's program and in the worst case require 14 bytes in the stack including the two bytes used by the call which invokes the function routine.

In every case return is made to the byte immediately following the last parameter value (if any). The return address generated by the call is used as a parameter list pointer

LEGEND:

Throughout this narrative and program comments certain abbreviations have been utilized, hopefully with a high degree of consistency. Most of these abbreviations and symbols are self explanatory; however, in the interest of clarity they are explained below.

A(X)	16 bit address of X.
DB	Data byte, 8 bits, operand is value.
DRXY	Double register pair XY.
DW	Data word, 16 bits, operand is value.
HOB	High order byte of 16 bit address.
ICV	An immediate character value.
LOB	Low order byte of 16 bit address.
PLAD	Parameter list address.
SIZ	The size/length of an operand.
SRX	Single register X.
TOS	Top of stack.
UDRXY	User's double register pair XY contents.
USRRET	Return point in the user's program.
USRX	User's single register X contents.
X → Y	Contents of X moved to Y.
xxx yyy zzz	Arbitrary instructions.
<*>	Resident page number of the utility routines.

Listing 1, continued:

Split Octal Address	Octal Code	Label	Op	Operand	Commentary
<*> 135	343	SASIX	XTHL		UDRHL to TOS; FRRET=FRCOMMAND address to TOS;
<*> 136	042 155 <*>		SHLD	SASIC+1	Store FRCOMMAND address in CALL;
<*> 141	341		POP	H	TOS=UDRHL to DRHL clear return;
<*> 142	343		XTHL		UDRHL to TOS; USRRET=PLAD to DRHL;
<*> 143	315 000 <*>		CALL	SASNT	Call SASNT to load parameters;
<*> 146	343		XTHL		USRRET=PLAD+3 to DRHL; FDRHL to TOS;
<*> 147	176		MOV	A,M	Immediate character value to SRL;
<*> 150	043		INX	H	Incr USRRET=PLAD (+4 immed group);
<*> 151	343		XTHL		True USRRET to TOS; FDRHL to DRHL;
<*> 152	157		MOV	L,A	Move ICV to SRL;
<*> 153	032	SASIL	LDAX	D	Indexed FIELD char to SRA;
<*> 154	315 000 000	SASIC	CALL	Q'000000'	CALL the execution commands;
<*> 157	022		STAX	D	Store result in indexed FIELD;
<*> 160	023		INX	D	Incr FIELD address index;
<*> 161	045		DCR	H	Decrement length/size;
<*> 162	302 153 <*>		JNZ	SASIL	Loop until count is zero;
<*> 165	303 062 <*>		JMP	FRXIT	Jump to funct routine exit logic;
<*> 170	315 135 <*>	NICH	CALL	SASIX	CALL SASIX execution control rtn passing address of following;
<*> 173	245		ANA	L	Logical AND SRL=ICV to SRA;
<*> 174	311		RET		Return to SASIX;
<*> 175	315 135 <*>	OICH	CALL	SASIX	See NICH comment at address 170;
<*> 200	265		ORA	L	Logical OR SRL to SRA;
<*> 201	311		RET		Return to the SASIX routine;
<*> 202	315 135 <*>	XICH	CALL	SASIX	See NICH comment at address 170;
<*> 205	255		XRA	L	Logical XOR SRL to SRA;
<*> 206	311		RET		Return to SASIX;
<*> 207	315 135 <*>	MVICH	CALL	SASIX	See NICH comment at address 170;
<*> 212	175		MOV	A,L	Move SRL to SRA;
<*> 213	311		RET		Return to SASIX;
<*> 214	343	VALFX	XTHL		UDRHL to TOS; FRRET=FRCOMMAND address to DRHL;
<*> 215	042 227 <*>		SHLD	VALFC+1	Store FRCOMMAND address in CALL;
<*> 220	341		POP	H	TOS=UDRHL to DRHL clear return;
<*> 221	343		XTHL		UDRHL to TOS; USRRET=PLAD to DRHL;
<*> 222	315 000 <*>		CALL	SASNT	Call SASNT to load parameters;
<*> 225	032	VALFL	LDAX	D	Indexed FIELD character to SRA;
<*> 226	315 000 000	VALFC	CALL	Q'000000'	CALL the execution commands;
<*> 231	302 062 <*>		JNZ	FRXIT	If character not valid exit;
<*> 234	023		INX	D	Incr FIELD address index;
<*> 235	045		DCR	H	Decrement length/size;
<*> 236	302 225 <*>		JNZ	VALFL	Loop until count is zero;
<*> 241	303 062 <*>		JMP	FRXIT	Jump to exit all chars valid;
<*> 244	315 214 <*>	VALAS	CALL	VALFX	CALL VALFX execution control rtn passing address of following;
<*> 247	376 040	VALAC	CPI	Q'040'	Is SRA a space?
<*> 251	310		RZ		Return to VALFX if equal;
<*> 252	376 101	VALAO	CPI	Q'101'	Is SRA an 'A'?
<*> 254	330		RC		Return to VALFX if less than 'A';
<*> 255	376 132		CPI	Q'132'	Is SRA a 'Z'?
<*> 257	310	VALXT	RZ		Return to VALFX if equal;
<*> 260	320		RNC		Return to VALFX if greater;
<*> 261	277		CMP	A	Compare SRA to SRA force Z=1;
<*> 262	311		RET		Return to VALFX char is valid;
<*> 263	315 214 <*>	VALNS	CALL	VALFX	See VALAS comment at addr 244;
<*> 266	376 060	VALNC	CPI	Q'060'	Is SRA a '0'?
<*> 270	330		RC		Return to VALFX if less;
<*> 271	376 071		CPI	Q'071'	Is SRA a '9'?
<*> 273	303 257 <*>		JMP	VALXT	Jump to validation exit logic;
<*> 276	315 214 <*>	VALOS	CALL	VALFX	See VALAS comment at addr 244;
<*> 301	376 060	VALOC	CPI	Q'060'	Is SRA a '0'?
<*> 303	330		RC		Return to VALFX if less;
<*> 304	376 067		CPI	Q'067'	Is SRA a '7'?
<*> 306	303 257 <*>		JMP	VALXT	Jump to validation exit logic;
<*> 311	315 214 <*>	VALXS	CALL	VALFX	See VALAS comment at addr 244;
<*> 314	315 247 <*>	VALXC	CALL	VALAC	Call VALAC utility routine;
<*> 317	310		RZ		Return to VALFX if alphabetic;
<*> 320	315 266 <*>		CALL	VALNC	Call VALNC utility routine;
<*> 323	311		RET		Return to VALFX;
<*> 324	315 214 <*>	VALHS	CALL	VALFX	See VALAS comment at addr 244;
<*> 327	315 266 <*>	VALHC	CALL	VALNC	Call VALNC utility routine;
<*> 332	310		RZ		Return to VALFX if numeric;
<*> 333	376 101		CPI	Q'101'	Is SRA an 'A'?
<*> 335	330		RC		Return to VALFX if less;
<*> 336	376 106		CPI	Q'106'	Is SRA an 'F'?
<*> 340	303 257 <*>		JMP	VALXT	Jump to validation exit logic;
<*> 343	343	MVSYM	XTHL		UDRHL to TOS; USRRET=PLAD to DRHL;
<*> 344	315 010 <*>		CALL	DASNT	Call DASNT function entry rtn;
<*> 347	343		XTHL		USRRET=PLAD+5 to DRHL; FDRHL to TOS;
<*> 350	176		MOV	A,M	Move stop char to SRA;
<*> 351	043		INX	H	Incr USRRET=TRUERET=PLAD+6;
<*> 352	343		XTHL		True USRRET to TOS; FRDHL to DRHL;
<*> 353	157		MOV	L,A	Move stop char from SRA to SRL;
<*> 354	345		PUSH	H	DRHL to TOS for length moved calc;
<*> 355	032	MVSYL	LDAX	D	Indexed FIELD2 char to SRA;
<*> 356	275		CMP	L	Compare it to stop char;
<*> 357	312 371 <*>		JZ	MVSYX	If equal go to MVSYM exit logic;
<*> 362	002		STAX	B	Else store in indexed FIELD1;
<*> 363	003		INX	B	Incr FIELD1 address index;
<*> 364	023		INX	D	Incr FIELD2 address index;
<*> 365	045		DCR	H	Decrement length/size;
<*> 366	302 355 <*>		JNZ	MVSYL	Loop until count is zero;
<*> 371	361	MVSYX	POP	PSW	DRHL from 354 is popped SRA=len;
<*> 372	224		SUB	H	Subtr remaining len = moved len;
<*> 373	341		POP	H	True USRRET to DRHL;
<*> 374	301		POP	B	UDRPSW&A discarded by this pop;
<*> 375	303 065 <*>		JMP	FRXT2	Exit skipping SRA restore;

and is incremented by the function routines to effect a proper return upon completion of the requested function.

In addition to the specific function routines there are several support routines which are used by the function routines for entry and exit logic. These support routines can be used by the programmer in developing his or her own coded function routines provided that entry to the user coded function routines is identical in form to the function routine entry logic used in this package.

Whenever one sets out to design and develop a piece of software it is extremely important that the design parameters be defined in advance and that the tradeoffs be understood and evaluated. In the case of the BARC 8080 character and string manipulation utility routines, memory space was judged to be of greater importance than execution time. The design parameters for this software package were:

1. To pack as many functions as possible in as little space as possible regardless of the impact upon execution times.
2. Not to use over 256 bytes.
3. To provide as much flexibility as possible within the requirements of 1 and 2.
4. To provide a high degree of user convenience.

What follows is a description of the function and purpose of every usable function and support routine in the package and how to use each. The routines are described in alphabetical order by name. Listing 1 gives the code for all the routines, and table 1 summarizes the routines and entry points.

Name	Address	Function
CLCHR	<*> 123	Compare FIELD1 contents to FIELD2 contents;
DASNT	<*> 010	Double address plus size function entry routine;
DASXR	<*> 034	Double address plus size function execution support routine;
FRXIT	<*> 062	Function routine exit logic;
MVCHR	<*> 110	Move FIELD2 contents to FIELD1;
MVICH	<*> 207	Fill FIELD with immediate character value;
MVSYM	<*> 343	Move FIELD2 contents to FIELD 1 terminating on stop character;
NCHR	<*> 071	Logical AND MASK to FIELD;
NICH	<*> 170	Logical AND immediate character value to all bytes in FIELD;
OCHR	<*> 076	Logical OR MASK to FIELD;
OICH	<*> 175	Logical OR immediate character value to all bytes in FIELD;
SASIX	<*> 135	Single address, size and immed function execution support routine;
SASNT	<*> 000	Single address plus size function entry routine;
SWCHR	<*> 115	Swap contents of FIELD1 with contents of FIELD2;
VALAC	<*> 247	Validate alphabetic character;
VALAS	<*> 244	Validate alphabetic string of characters;
VALFX	<*> 214	Validate string function execution support routine;
VALHC	<*> 327	Validate hexadecimal character;
VALHS	<*> 324	Validate hexadecimal string of characters;
VALNC	<*> 266	Validate numeric character;
VALNS	<*> 263	Validate numeric string of characters;
VALOC	<*> 301	Validate octal character;
VALOS	<*> 276	Validate octal string of characters;
VALXC	<*> 314	Validate alphanumeric character;
VALXS	<*> 311	Validate alphanumeric string of characters;
VALXT	<*> 257	Validate string function exit logic;
XCHR	<*> 103	Logical exclusive OR MASK to FIELD;
XICH	<*> 202	Logical exclusive OR immediate character value to all bytes in FIELD;

Table 1: Alphabetical listing of BARC utility routines and their entry points. The low order addresses refer to listing 1.

CLCHR: Compare Logical Characters

The CLCHR utility routine compares two character strings byte by byte from left to right and terminates upon encountering the first inequality. The condition flags are set according to the relationship of the contents of FIELD1 to the contents of FIELD2. The possible combinations are:

```
FIELD1 = FIELD2   Z=1,  CY=0
FIELD1 < FIELD2   Z=0,  CY=0
FIELD1 > FIELD2   Z=0,  CY=1
```

Both strings must be of the same length and may be up to 256 bytes long. The calling sequence for this utility routine is:

```
CALL  CLCHR      Call CLCHR utility routine;
DW    A(FIELD1)  FIELD1 address;
DW    A(FIELD2)  FIELD2 address;
DB    SIZ        Length of fields where 0 means a length of 256;
```

DASNT: Double Address plus Size, Function Entry Support Routine

The DASNT support routine is used to save the user's register contents and load the parameters following the original user's utility routine call. This routine is called by the function execution routine which was called by the user. The calling sequence for this support routine is:

```
XTHL              UDRHL to TOS; USRRET to DRHL;
CALL    DASNT     Call DASNT routine;
```

Upon return from the DASNT support routine the user's registers have been saved on the stack and the working registers contain the following:

DRBC = First address parameter following user's call.
DRDE = Second address parameter following user's call.
SRH = Length parameter.
TOS = True user's return point to byte following parameters.

Exit from a function routine which has used DASNT should only be effected by jumping to the FRXIT routine.

DASXR: Double Address plus Size, Function Execution Support Routine

The DASXR support routine is used as a generalized execution routine for the various functions which require two address parameters and a size parameter, operate on the data from left to right and replace the contents of the first operand with the result. (**Note:** Both fields must be of the same length and may be up to 256 bytes long.) DASXR simply controls the execution of the function by performing the housekeeping and looping involved in controlling the execution. DASXR uses DASNT as its entry logic to preserve the contents of the user registers and to load the parameter values into the working registers. On each iteration of the loop in DASXR it loads the next byte of FIELD2 into SRL and the next byte of FIELD1 into SRA (the accumulator) before turning control over to the logic which will operate on the data. DASXR increments the addresses of the fields and loops until the count is consumed or until the calling program terminates its operation. Exit from DASXR is through the FRXIT exit logic which restores the user registers, with the exception of the program counter and flags, to their original contents. Here's an example of the use of DASXR as the controlling logic for an addition routine where the operands are stored least significant byte first:

1. In line coding in user program

```
CALL   USRTN       Call user written ADD logic;
DW     A(FIELD1)   Address of augend and sum;
DW     A(FIELD2)   Address of addend;
DB     SIZ         Length of fields where 0 means a length of 256;
```

2. Subroutine in user program called by 1 above

```
USRTN  ORA  A      Clear carry;
       CALL DASXR  Call DASXR support routine;
       ADC  L      Add SRL and CARRY to accumulator;
       DAA         (Decimal adjust only if data is decimal);
       RET         Return to DASXR support routine;
```

3. If a premature or abnormal termination of the loop is required as in the CLCHR function routine it should take the following form:

```
USRTN  xxx               Setup instructions, if any;
       CALL     DASXR    Call DASXR support routine;
       yyy               Function execution instructions
       yyy                  as required;
       R(cond)           Conditional return to DASXR to continue;
       zzz               Instructions to be executed if the condition
       zzz                  is not met;
       POP      H        Clear return address to DASXR from stack;
       JMP      FRXIT    Jump to the function exit logic for
                            abnormal or premature return;
```

The calls to DASXR in 2 and 3 are not used as calls to which a return will be made. They are used to pass the address of the function execution instructions which follow the calls to the DASXR support routine. DASXR stores the passed address of the function execution instructions in the address portion of a call instruction within itself and executes the call within itself once for each iteration of the control loop.

It is very important to realize that the call to DASXR cannot be inline in the coding but must be called by the logic which is called by the inline parameter passing call if it is to function correctly.

FRXIT: Function Routine Exit Logic

The FRXIT routine is used to restore the contents of the original user's registers and to return to the proper address location, following the parameters of the original user's call. FRXIT should always be used when exiting from a function routine which utilized the DASNT or SASNT function entry routines. This logic is entered by jumping to it unconditionally or conditionally when it is desired to return to the original caller. No other commands are required prior to the jump to prime this routine. All registers except the program counter and flags are restored to their original contents prior to returning; the flags are returned to the caller as set by the function execution routine.

MVICH: Move Character Immediate (Character Fill)

The MVICH utility routine will move a specified byte value known as the immediate character value (ICV), to every byte location in a specified field. The specified field may be up to 256 bytes long. The calling sequence for this utility routine is:

```
CALL  MVICH     Call MVICH utility routine;
DW    A(FIELD)  Address of the receiving field;
DB    SIZ       Length of the field where 0 means a length of 256;
DB    ICV       Immediate character value;
```

MVCHR: Move Characters

The MVCHR utility routine will move a character string up to 256 bytes long from one location to another. The format of the calling sequence for this utility routine is:

```
CALL  MVCHR       Call MVCHR utility routine;
DW    A(DESTIN)   Address of the destination field;
DW    A(SOURCE)   Address of the source field;
DB    SIZ         Length of the fields where 0 is the length code for 256;
```

MVSYM: Symbolic Move

The MVSYM utility routine will move a character string up to 256 bytes long from one location to another and stop moving when one of two conditions is met:

1. A character from the sending area is encountered which is equal in value to the ICV known as the stop character (**Note:** The stop character is *not* moved).

or

2. The entire string has been moved according to the specified size and no character was found which was equal in value to the ICV stop character.

In either event when return is made to the user the accumulator (SRA) contains a count of the characters moved. Caution must be exercised when strings of length 256 are moved using MVSYM because if the first character in the string is a stop character, the length moved will be zero and when 256 characters are moved without encountering a stop character, the length moved will also be zero since the size value for 256 is zero; therefore, whenever the length moved for a field which is 256 bytes long is zero, test the first character in the source field to determine if it is a stop character. If it is, then the length moved is really zero, otherwise the length moved is 256. The calling sequence for the MVSYM utility routine is:

CALL	MVSYM	Call MVSYM utility routine;
DW	A(DESTIN)	Address of the destination field;
DW	A(SOURCE)	Address of the source field;
DB	SIZ	Max length for the move where 0 means a length of 256;
DB	ICV	The immediate character value is the stop character;

OCHR: Logical OR Character Strings

The OCHR utility routine will logically OR a character string called MASK to another character string called the FIELD; the result will replace the contents of the FIELD. Both strings must be of the same length and may be up to 256 bytes long. The calling sequence for this utility routine is:

CALL	OCHR	Call OCHR utility routine;
DW	A(FIELD)	Address of the FIELD;
DW	A(MASK)	Address of the MASK;
DB	SIZ	Length of the fields where 0 means a length of 256;

OICH: Logical OR Characters Immediate

The OICH utility routine will logically OR a specified byte value known as the immediate character value (ICV) to every byte location in a specified FIELD. The specified FIELD may be up to 256 bytes long. The calling sequence for this utility routine is:

CALL	OICH	Call OICH utility routine;
DW	A(FIELD)	Address of the FIELD;
DB	SIZ	Length of the FIELD where 0 means a length of 256;
DB	ICV	Immediate character value;

NCHR: Logical AND Character Strings

The NCHR utility routine will logically AND a character string called MASK to another character string known as the FIELD; the result will replace the contents of FIELD. Both strings must be of the same length, which may be up to 256 bytes. The calling sequence for this utility routine is:

CALL	NCHR	Call NCHR utility routine;
DW	A(FIELD)	Address of the field string;
DW	A(MASK)	Address of the mask string;
DB	SIZ	Length of the fields where 0 means a length of 256;

NICH: Logical AND Characters Immediate

The NICH utility routine will logically AND a specified byte value known as the immediate character value (ICV) to every byte location in a specified FIELD. The specified FIELD may be up to 256 bytes long. The calling sequence for this utility routine is:

CALL	NICH	Call NICH utility routine;
DW	A(FIELD)	Address of FIELD;
DB	SIZ	Length of FIELD;
DB	ICV	Immediate character value;

SASIX: Single Address, Size and Immediate Character, Function Execution Support Routine

The SASIX support routine is used as a generalized execution routine for the various functions which require one address parameter, a size parameter for one to 256 bytes, and an immediate character value which is used to operate upon the contents of the field, operate on the data from left to right and replace the contents of the field with the result. SASIX does not actually perform the required function; that is the responsibility of the programmer who is using SASIX. SASIX simply controls the execution of the function by performing the housekeeping and looping involved in controlling the execution. SASIX uses SASNT as its entry logic to preserve the contents of the user registers and to load the parameters into the working registers. The immediate character value is loaded into SRL and retained there until altered by the programmer. On each iteration of the loop in SASIX it loads the next byte of the field into accumulator before turning control over to the logic which will operate on the data. SASIX increments the address of the field and loops until the count is consumed or until the programmer busts out of its control. Exit from SASIX is through the FRXIT exit logic which restores the user registers with the exception of the program counter and flags to their original contents. An example of the use of SASIX as the controlling logic for a routine which translates all the spaces in a field to zeros is as follows:

SASIX, continued

1. Inline coding in user program:

```
CALL  USRTN     Call user written logic;
DW    A(FIELD)  Address of field to be translated;
DB    SIZ       Length of field to be translated;
DB    ' '       Immediate character value of a space;
```

2. Subroutine in user program called by the above sequence:

```
USRTN  CALL  SASIX   Call SASIX support routine;
       CMP   L       Compare immediate character value (in SRL) to accumulator;
       RNZ           Return to SASIX if not equal;
       MVI   A,'0'   Move immediate value of character '0' to accumulator, replacing
                        occurrence of the immediate character value;
       RET           Return to SASIX;
```

3. Should an abnormal or premature return be required, for example, in a situation such as in 2 above where it is desired to translate only the leading spaces into zeros and then stop, it should take the following form:

```
USRTN  XXX           Setup instructions, if any;
       CALL  SASIX   Call SASIX utility routine;
       CMP   L       Compare SRL to accumulator;
       MVI   A,'0'   Move a character zero to accumulator to replace
                        immediate character value;
       RZ            Return to SASIX if accumulator is equal to the
                        immediate character value;
       POP   H       Else clear return to SASIX from stack;
       JMP   FRXIT   Jump to exit logic before count is zero;
```

The calls to SASIX above are not used as calls to which a return will be made. They are used to pass the address of the function execution instructions which follow the calls to the SASIX support routine. SASIX stores the passed address of the function execution instructions in the address portion of a call instruction within itself and executes the call within itself once for each iteration of the control loop.

It is very important to realize that the call to SASIX cannot be inline in the coding but must be called by the logic which is called by the inline parameter passing call if it is to function correctly.

SASNT: Single Address Plus Size, Function Entry Routine

The SASNT routine is used to save the user register contents and load the parameters following the original user's utility routine call. This routine is called by the function execution routine which was called by the user. The calling sequence for this support routine is:

```
XTHL            UDRHL to TOS; USRRET to DRHL;
CALL   SASNT    Call SASNT support routine;
```

Upon return from the SASNT support routine the user's register contents have been saved on the stack and the working registers contain the following:

```
DRDE  =  Address parameter following user's call;
SRH   =  Length or size parameter;
TOS   =  True user's return point to byte following parameters;
```

Exit from a function execution routine which has used SASNT should only be effected by jumping to the FRXIT routine which is described above.

SWCHR: Swap Character Strings

The SWCHR utility routine will swap two character strings. The contents of FIELD1 replace the contents of FIELD2 while the contents of FIELD2 are replacing the contents of FIELD1. This routine can be used when writing internal sort routines. Both strings must be of the same length and may be up to 256 bytes long. The calling sequence for the SWCHR routine is:

```
CALL  SWCHR      Call SWCHR utility routine;
DW    A(FIELD1)  Address of one of the fields to be swapped;
DW    A(FIELD2)  Address of the other field to be swapped;
DB    SIZ        Length of the fields where 0 means a length of 256;
```

VALAC: Validate Alphabetic Character

The VALAC utility routine tests the character in the accumulator to determine if it is an alphabetic character or a space. Upon return, if the ZERO flag is equal to a 1, the character is valid as tested; if the ZERO flag is 0, it is invalid. The calling sequence for this routine is:

```
CALL  VALAC  Call VALAC utility routine;
```

VALAS: Validate Alphabetic Character String

The VALAS routine tests the characters in a specified string to determine if they are all alphabetic characters or spaces. Examination proceeds from left to right one byte at a time; the routine terminates if an invalid character is found. Upon return, the Z flag is 1, all characters in the string satisfied the validation requirements; otherwise the Z flag is 0. The calling sequence for this utility routine is:

```
CALL  VALAS     Call VALAS utility routine;
DW    A(FIELD)  Address of the string to be tested;
DB    SIZ       Length of the field to be tested;
```

VALFX: Validate String, Function Execution Support Routine

The VALFX support routine is used as a generalized execution routine for the various string validation functions. These functions require a single address parameter for the field to be validated and a size parameter which specifies the length of the field which may be up to 256 bytes long. The contents of the field are not changed. VALFX does not actually perform the required function, for that is the responsibility of the programmer who is using VALFX. VALFX simply supplies the characters in the field one at a time, starting with the lefthand end, in the accumulator and controls the execution of the function by performing the housekeeping and looping involved in controlling the execution. VALFX increments the address of the field and loops until the count is consumed or the character which is invalid to the test is encountered. If the programmer who has coded the test logic returns to VALFX with a Z flag value of 1, VALFX will supply the next character in the string; otherwise it terminates execution and exits via FRXIT to the calling point with a Z flag value of 0. If all characters in the string were valid, return is made to the calling point with the Z flag equal to 1 via FRXIT. VALFX uses SASNT as its entry logic to preserve the contents of the user registers and to load the parameters into the working registers; FRXIT is used as the exit logic to restore the user registers, with the exception of the program counter and flags, to their original contents. An example of the use of VALFX as the controlling logic for a routine which validates that all of the characters in a field are letters of the Greek alphabet, as implemented on the Digital Group System, would be as follows:

1. Inline coding in user program:

```
CALL  USRTN      Call user written logic;
DW    A(FIELD)   Address of field to be validated;
DB    SIZ        Length of field to be validated where 0 means a length of 256;
```

2. Subroutine in user program called by 1 above:

```
USRTN  CALL  VALFX  Call VALFX function execution routine;
       CPI   'α'    Compare accumulator to a Greek alpha;
       RC           Return if accumulator less;
       CPI   'Ω'    Compare accumulator to an omega, end of Greeks;
*      RZ           Return if accumulator equal to omega, valid;
*      RNC          Return if accumulator greater than omega, invalid;
*      CMP   A      Force Z=1, if 'α' <= accumulator <= 'Ω'; valid;
*      RET          Return to VALFX with valid conditions;
```

Note: For range of value tests like this one the instructions marked with asterisks (*) above may be replaced by the following instruction which jumps to an identical instruction sequence within the validation utility routines:

```
JMP   VALXT   Jump to the validation test logic;
```

3. If it were desired to determine that the field to be validated contained only Greek alphas and omegas and nothing else, the subroutine in the user program called by 1 above would be as follows:

```
USRTN  CALL  VALFX  Call VALFX function execution routine;
       CPI   'α'    Compare accumulator to an alpha;
       RZ           Return if equal;
       CPI   'Ω'    Compare accumulator to an omega;
       RET          Return to VALFX with conditions set;
```

The preceding calls to VALFX are not used as calls to which a return will be made. They are used to pass the address of the function execution instructions which follow the calls to the VALFX support routine. VALFX stores the passed address of the function execution instructions in the address portion of a call instruction within itself and executes that call once for each iteration of the control loop.

It is very important to realize that the call to VALFX cannot be inline in the coding but must be called by the logic which is called by the inline parameter passing CALL if it is to function correctly.

VALHC: Validate Hexadecimal Digit Character

The VALHC routine tests the character in the accumulator to determine if it is one of the 16 characters (0 to 9 or A to F) which are used to represent radix 16 (hexadecimal) digits. Upon return, if the Z flag is 1, the character in the accumulator is a hexadecimal digit; otherwise Z is 0. The calling sequence for this utility routine is:

```
CALL   VALHC   Call VALHC utility routine;
```

VALHS: Validate Hexadecimal Digit String

The VALHS routine tests the characters in a specified string to determine if they are all valid hexadecimal digits. Examination proceeds from left to right one byte at a time; the routine terminates if an invalid character is found. Upon return, if the Z flag is 1, all characters in the string were hexadecimal digits; otherwise the Z flag is 0. The calling sequence for this utility routine is:

```
CALL  VALHS      Call VALHS utility routine;
DW    A(FIELD)   Address of the field to be validated;
DB    SIZ        Length of the field where 0 means a length of 256;
```

VALNC: Validate Numeric Character

The VALNC routine tests the character in the accumulator to determine if it is one of the digits in the decimal numbering system. Upon return, if the Z flag is 1, the character in the accumulator is one of the digits 0 through 9, otherwise the Z flag is 0. The calling sequence for this utility routine is:

```
CALL   VALNC   Call VALNC utility routine;
```

VALNS: Validate Numeric String

The VALNS routine tests the characters in a specified string to determine if they are all valid decimal digits. Examination proceeds from left to right one byte at a time; the routine terminates if an invalid character is found. Upon return, if the Z flag is 1, all of the characters in the field were valid decimal digits; otherwise the Z flag is 0. The calling sequence for this utility routine is:

```
CALL   VALNS      Call VALNS utility routine;
DW     A(FIELD)   Address of the field to be validated;
DB     SIZ        Length of the field where 0 means a value of 256;
```

VALOC: Validate Octal Character

The VALOC routine tests the character in the accumulator to determine if it is one of the digits in the octal numbering system. Upon return, if the Z flag is 1, the character in the accumulator is a valid octal digit; otherwise Z is 0. The calling sequence for this utility routine is:

```
CALL   VALOC   Call VALOC utility routine;
```

VALOS: Validate Octal String

The VALOS routine tests the characters in a specified string to determine if they are all valid octal digits. Examination proceeds from left to right one byte at a time; the routine terminates if an invalid character is found. Upon return, if the Z flag is 1, all characters in the string were found to be valid octal digits; otherwise Z is set to 0. The calling sequence for this utility routine is:

```
CALL   VALOS      Call VALOS utility routine;
DW     A(FIELD)   Address of the field to be validated;
DB     SIZ        Length of the field where 0 means a length of 256;
```

VALXC: Validate Alphanumeric Character

The VALXC routine tests the character in the accumulator to determine if it is one of the characters A to Z, 0 to 9, or space. Upon return, if the Z flag is equal to 1, the character in the accumulator satisfied the validity requirements; otherwise Z is set to 0. The calling sequence for this utility routine is:

```
CALL   VALXC   Call VALXC utility routine;
```

VALXS: Validate Alphanumeric String

The VALXS routine tests the characters in a specified string to determine if they are all alphabetics, numerics or spaces. Examination proceeds from left to right one byte at a time; the routine terminates if an invalid character is encountered. Upon return, if the Z flag is equal to 1, all of the characters in the string satisfied the test conditions; otherwise Z is set to 0. The calling sequence for this utility routine is:

```
CALL   VALXS      Call VALXS utility routine;
DW     A(FIELD)   Address of the field to be validated;
DB     SIZ        Length of the field where 0 means a length of 256;
```

VALXT: Validate Test Function Exit Logic

The VALXT logic is used to set the condition codes when a validation test is testing for a closed range of values. This routine is entered by a jump command immediately following the upper limit compare, assuming of course that the upper limit is tested last. VALXT forces the Z flag to have a value of 1 when the tested character falls within the range. See the example given in the VALFX routine description.

XCHR: Logical Exclusive OR Characters

The XCHR utility routine will logically exclusive OR a character string known as the MASK to another character string known as the FIELD; the result will replace the contents of the field. Both strings must be of the same length and may be up to 256 bytes long. The calling sequence for this utility routine is:

```
CALL   XCHR       Call XCHR utility routine;
DW     A(FIELD)   Address of the FIELD and the result;
DW     A(MASK)    Address of the MASK string;
DB     SIZ        Length of the fields where 0 means a length of 256;
```

XICH: Logical Exclusive OR Characters Immediate

The XICH utility routine will logically exclusive OR a specified byte value known as the immediate character value (ICV) to every byte location in a specified field. The specified field may be up to 256 bytes long. The calling sequence for this utility routine is:

```
CALL   XICH       Call XICH utility routine;
DW     A(FIELD)   Address of the field;
DB     SIZ        Length of the field where 0 means a length of 256;
DB     ICV        Immediate character value; ■
```

Continued from page 4

Computeritis: the infection of the imagination with ideas about "what neat things could be done with a computer if only I had access."

At first, personal computing people were very technical types... now we find a sprinkling of lawyers, doctors, kids, retirees, art teachers, tavern owners, and others.

were nearly all very technical types – engineers, programmers, and electronics buffs. But times are changing very rapidly in personal computing. Now we find a sprinkling of lawyers, doctors, kids, retirees, art teachers, and tavern owners. Less and less technical expertise is needed. In fact, with computer stores ready to help and with assembled kits readily available, one can get by with no hardware expertise. And we all know that BASIC (the programming language most widely available with personal computers) has been taught widely in high schools – so very little in the way of prior background is needed. Rather, what's needed is a little bread and a lot of curiosity about one of the most curious of mankind's inventions.

Why does an individual buy his or her own computer? I think there are three primary reasons: (1) he or she has a specific application that he or she wants to implement; (2) he or she is curious and wants to learn about computers; and, (3) his or her future job security may depend on his or her knowing about computers.

Among the people wanting to implement a specific application are many small, usually one-person, businesses. There is a sprinkling of people with really innovative applications such as devices to provide assistance to a handicapped individual. Among those who want to learn about computers are the naturally very curious people who in the past would have pursued other electronics-oriented hobbies such as ham radio. There are a surprisingly large number of people who can greatly increase their job security with a little knowledge of computers – even people in fields seemingly not related to computers.

Owning the computer does not, by itself, provide a person with all that's needed to learn about computers. There is a major educational process that must be "endured." The needed information can be gleaned from many sources without resorting to formal education: books, magazines, and, through clubs and conventions, other people.

One of the primary means of obtaining information has been computer clubs. There are nearly 150 computer clubs in the United States and a few in Canada and other countries. Club sizes vary from a handful to Southern California Computer Society's more than 5,000 members. These clubs are not affiliated in any way with one another except that a few clubs are regional and have several local chapters.

The primary activity of most computer clubs is the regular meeting. Typically, a club meets with a frequency of from every two weeks to once a month. The object of a meeting may simply be the informal exchange of information by club members. There may be a presentation by a guest speaker, a demonstration of a product or a project, or a workshop on some particular subject. It is not unusual for several people to show up unexpectedly with computer projects to show. Whatever the main objective, some side activities always take place: Individuals share their experiences and insights – usually with enthusiasm reminiscent of a revival testimonial.

Many clubs publish newsletters which are avidly read by the club members. In fact, some of the newsletters are so good that they have many subscribers outside the club's primary geographic area. The newsletters contain articles on the activities of the club, information on new products, schematics for new widgets, program listings, experiences of club members with various products, and a wealth of other information wanted by personal computing enthusiasts. Although the newsletters vary in production quality from computer listings all the way to glossy magazine format, a typical newsletter is a few Xeroxed pages.

Clubs are beginning to exchange newsletters which may bring about improved communication and some coordination of activities among clubs. A big question arises as to whether or not a national federation of clubs will form. On one hand, a national federation could benefit its members by providing publications, improved information exchange, sponsorship of conferences, encouragement of product standards, software exchange, and protection of its members in dealing with product suppliers. On the other hand, many people believe that a formal organization would be counterproductive to the goal of most computer clubs; namely, the free exchange of information for the benefit of the members. In fact, some clubs, even very large clubs, elect no officers, collect no dues, and claim no members. The newsletter is funded by passing a hat when the treasury gets low.

The personal computing movement is held together nationally by the magazines. There are a surprising number of high quality publications. Heading the list is BYTE which not only publishes a wide variety of technical articles of interest to personal computing folks, but also provides a wide assortment of other goodies such as new product announcements, book reviews, and news coverage of personal computing conferences. Among several other publica-

tions, each has its own unique orientation. *Interface Age*, a general hobbyist publication, started as the newsletter of the Southern California Computer Society, but is now published independently. The stated mission of *Dr Dobb's Journal of Calisthenics and Orthodontia* is to foster the free exchange of software. One has only to look at the creation of Tiny BASIC to realize the incredible success that *Dr Dobb's* has had in accomplishing its goal. David Ahl's *Creative Computing* is oriented toward the use of computer games by kids as an educational vehicle. *People's Computer Company* is published in newsletter format, is largely oriented towards kids, but has significant personal computing coverage. Several other established publications such as *Popular Electronics* and *Radio Electronics* feature major sections devoted to personal computing.

Any discussion of the personal computing movement would not be complete without mention of the major conferences. The first major conference was the MITS World Altair Convention held one weekend in March 1976 in Albuquerque NM. Although it was supposedly an Altair users' conference, when one wandered around the lobby of the hotel, the feeling of a big computer club meeting was very strong; and the fact that MITS was the organizer was really incidental. In attendance were nearly 1,000 people from across the country with a few international visitors.

Owning a computer does not by itself provide a person with all that's needed to learn about computers. There is a major educational process that must be "endured" in order to reap the rewards of computing in one's personal life.

The next major milestone was Personal Computing 76 held during August 1976 in Atlantic City NJ. The conference was organized almost single handedly by John Dilks, with major contributions provided by Dave Jones and Jim Main. The conference started as a project of a ham radio club but soon outgrew all expectations, probably simply because a conference was needed. The very successful conference drew 88 exhibitors with 110 booths and nearly 5,000 attendees.

Several conferences will probably be held over the next year. One "must" coming event for personal computing enthusiasts is the 1977 National Computer Conference Personal Computing Fair and Exposition

Soon we will be waiting only for some clever and well financed company to package the Home Information Processing Center and thus create the consumer demand for this next major home appliance concept.

Expert guidance is usually available from the computer store... it is a place to turn for local help and instruction.

scheduled for June 13-16 in Dallas TX. The National Computer Conference is the world's largest computer conference, attracting over 250 exhibitors with more than 1,000 booths and drawing more than 25,000 attendees. Major personal computing activities are planned for the 1977 NCC including a Personal Computing Fair, a special exhibit area for personal computing products, a program of paper and panel sessions, and a Computer Club Congress.

Now let's turn our attention to the manufacturers who started and support the personal computing movement. What types of companies are producing personal computing products? Until very recently, the typical personal computing product manufacturer was a rather small company whose only product lines were in the personal computing area; for example, IMS Associates, Polymorphic Systems, Processor Technology and Cromemco. Companies that don't quite fit the personal computing specialization are MITS, Southwest Technical Products, and iCOM. Recently, several larger companies have been seen making moves into the personal computing market; namely, Texas Instruments, Intel, and Digital Equipment Corporation.

Although at first nearly all personal computing products were sold by mail order direct from the manufacturer, we see now an important new institution emerging — the retail computer store. Presently, there are over 250 computer stores in the United States *[based on the number of BYTE's direct dealer sales outlets]*. A computer store is not an electronics store or greenhouse that happens to stock computers. The best computer stores offer a wide variety of products and services for the computer hobbyist and small business, including several lines of computers, parts, peripherals, prototyping equipment, books, magazines, software, repair service, custom interfacing, and consulting. The typical computer store has on display several demonstration computing systems so that an individual can see and try before buying. The computer store concept offers several advantages to the purchaser over buying directly from the manufacturer at no additional cost. The purchaser need not deal with several manufacturers in order to reap the benefits of cost and feature comparisons. Expert guidance is usually available from the computer store. Local service is provided as well as answers to the myriad of questions sure to materialize when a person takes home his/her first computer.

Now that we have characterized the personal computing movement in terms of the people, their clubs and conventions, the magazines they read, and the manufacturers of personal computing products, let's turn our attention to the impact of personal computing and its future. Most importantly, personal computing is the *leading* edge of the sharing of computing power by large corporations and government with the people. Soon our homes will be full of computers quietly improving many types of consumer goods, including: ovens, sewing machines, stereos, televisions, automobiles, sprinkler systems and security systems.

More significantly, however, the Home Information Processing Center is emerging from the efforts of personal computing enthusiasts to use the computer to improve the quality of their everyday activities. The Home Information Processing Center will provide a central coordination facility for other home appliances, assistance in a myriad of personal business and record keeping tasks, interface with external systems such as bank electronic funds transfer systems and retail stores, endless entertainment with computer based games, individualized learning through computer assisted instruction for us and our children, partial replacement for the mail with a home to home telephone-based communication system, remote access by telephone to home control functions, and each home with clerical assistance such as text editing.

The public is being primed now for acceptance of the Home Information Processing Center. On the other hand, as mentioned before, many consumer goods are incorporating microprocessors as control components, so the public will start to think of the microcomputer as a rather ordinary device. On another front, video games are beginning to physically appear a lot like the Home Information Processing Center. Specifically, the games are using the television as an output device, some of them are using simple keyboards as input devices, and some use audio tape cassettes as a means of storing programs. From this video game to the Home Information Processing Center is a seemingly small step. The Home Information Processing Center would have the keyboard, the television, and the tape cassette in

addition to mass storage, such as a floppy disk, a hard copy output device, not very different from the ordinary typewriter, and be interfaced to the telephone line. The hardware technology for a low cost Home Information Processing Center exists. The application and software technology will grow from the personal computing movement. Soon we will be waiting only for some clever and well-financed company to package the product and create the consumer demand for this next major home appliance. When the Home Information Processing Center has become commonplace, personal computing will have grown to maturity.

What started as a hobby could well grow into a "necessity" of life.■

Names and addresses of some of the publications mentioned in this editorial:

Interface Age published by McPheters, Wolfe & Jones, 6515 Sunset Blvd, Suite 202, Hollywood CA 90028 (monthly).

Dr Dobb's Journal of Computer Calisthenics and Orthodontia, published by People's Computer Company, POB 310, Menlo Park CA 94025 (monthly).

Creative Computing, published by Ideametrics, POB 789-M, Morristown NJ 07960 (every two months).

People's Computer Company, published by People's Computer Company, POB 310, Menlo Park CA 94025 (published several times during the school year).

Popular Electronics, published by Ziff-Davis, widely available on newsstands (monthly).

Radio Electronics, published by Gernsback Publications Inc, widely available on newsstands (monthly).

The Word "Byte" Comes of Age. . .

We received the following from W Buchholz, one of the individuals who was working on IBM's Project Stretch in the mid 1950s. His letter tells the story.

Not being a regular reader of your magazine, I heard about the question in the November 1976 issue regarding the origin of the term "byte" from a colleague who knew that I had perpetrated this piece of jargon *[see page 77 of November 1976 BYTE, "Olde Englishe"]*. I searched my files and could not locate a birth certificate. But I am sure that "byte" is coming of age in 1977 with its 21st birthday.

Many have assumed that byte, meaning 8 bits, originated with the IBM System/360, which spread such bytes far and wide in the mid-1960s. The editor is correct in pointing out that the term goes back to the earlier Stretch computer (but incorrect in that Stretch was the first, not the last, of IBM's second-generation transistorized computers to be developed).

The first reference found in the files was contained in an internal memo written in June 1956 during the early days of developing Stretch. A byte was described as consisting of any number of parallel bits from one to six. Thus a byte was assumed to have a length appropriate for the occasion. Its first use was in the context of the input-output equipment of the 1950s, which handled six bits at a time. The possibility of going to 8 bit bytes was considered in August 1956 and incorporated in the design of Stretch shortly thereafter.

The first published reference to the term occurred in 1959 in a paper "Processing Data in Bits and Pieces" by G A Blaauw, F P Brooks Jr and W Buchholz in the *IRE Transactions on Electronic Computers*, June 1959, page 121. The notions of that paper were elaborated in Chapter 4 of *Planning a Computer System (Project Stretch)*, edited by W Buchholz, McGraw-Hill Book Company (1962). The rationale for coining the term was explained there on page 40 as follows:

> Byte *denotes a group of bits used to encode a character, or the number of bits transmitted in parallel to and from input-output units. A term other than* character *is used here because a given character may be represented in different applications by more than one code, and different codes may use different numbers of bits (ie, different byte sizes). In input-output transmission the grouping of bits may be completely arbitrary and have no relation to actual characters. (The term is coined from* bite, *but respelled to avoid accidental mutation to* bit.*)*

System/360 took over many of the Stretch concepts, including the basic byte and word sizes, which are powers of 2. For economy, however, the byte size was fixed at the 8 bit maximum, and addressing at the bit level was replaced by byte addressing. Since then the term byte has generally meant 8 bits, and it has thus passed into the general vocabulary.

Are there any other terms coined especially for the computer field which have found their way into general dictionaries of the English language?

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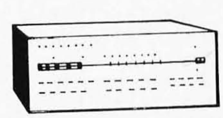
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About the Cover – Venus de Plotto

The unique drawing seen on this month's cover is an entry in the recent art contest, contributed by Arthur C Taber, 560 Rockdale Dr, San Francisco CA 94127. This piece of art was produced on equipment which is not exactly in the price range of the personal budget: Arthur does his art at the San Francisco State University computer center. The output device used to draw the figure was a CALCOMP 563 drum plotter which has a 30 inch (76 cm) drum and a resolution of 200 steps per inch (79 steps per cm). The computer used was a CDC 3150 which has 32 K 24 bit words. The 3150 can perform floating point calculations (eg: multiply or divide) in about 5 us, so the 9 ms per point which he timed on a wall clock represents 1800 equivalent floating point multiply operations per point.

The program used was an engineering simulation program which can be described metaphorically as "a highly distorted picture of four random rocks being thrown into a target whose viscosity varies from the center outward." In terms of the actual model, it is a high level language equation which describes a linear combination of damped harmonic oscillators in two dimensions, which is then rotated through a third dimension to produce a surface. The equation involved has two cosine terms, a square root term, and two exponential terms for damping. The plotting of this three dimensional surface was accomplished using a modified version of ACM algorithm number 483 for hidden line elimination, with a masking array of 10,000 words and the addition of some finesse. Finesse is defined as a random pen wiggle with an amplitude of several plotter steps, used to give texture and roughness to the lines in the original.

Can This Type of Art Be Done at Home (for Less than a Megabuck)?

The answer to the question is a qualified yes – this type of work can be done at home if the experimenter is willing to put together some of the required hardware, put up an Altair compatible machine with perhaps 16 K to 32 K of memory, and add a mass storage device such as a Phi-Deck or floppy disk which can be automatically run. In addition to this more or less "standard system" the would-be artist must acquire a plotter such as the $750 plotter kit described on page 85 of January 1977 BYTE, manufactured by Sylvanhills Laboratory Inc and a fast floating point unit such as the North Star Computers FPB, Model A, described on page 75 of January 1977 BYTE. Assuming the limiting factor is the floating point calculation speed, here is a quick feasibility estimate for the computation of Venus de Plotto.

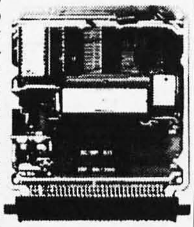
1. The original took a total of 1800 x 250,000 = 450 million calculations.

2. Allowing 111 us per floating multiply, the raw time requirement is:

$450 \times 10^6 \times 111 \times 10^{-6} = 49{,}950$ seconds

These numbers are very approximate, for they assume little IO was done in the original run, that all parts of the program would scale in the same way as the floating point multiply time, etc. However, with a personal computer, one has time to "burn" as it were. The liberating effects of the computer are quite obvious here: For this kind of art, one would (for example) set up the plotter and program some fine morning, go out and get the day's exercise (bicycling, cross country skiing, jogging, etc, depending on where you live and when), go to work, rendezvous with an intimate friend for dinner, check on the finished results, then spend a few minutes to modify the design parameters of the plot before retiring for the night with that smug self-satisfying feeling that comes from living a good life.■

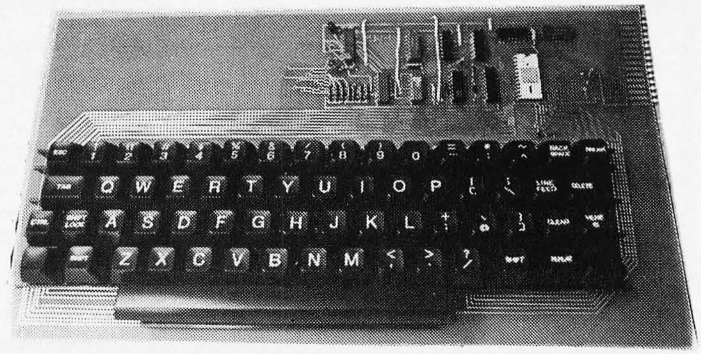
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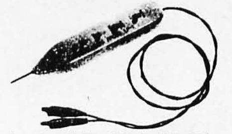
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A compact, versatile design and test tool for digital applications. By simply connecting the clip leads to the circuit power supply, setting the logic family switch to the proper position (TTL/DTL or CMOS) and touching the probe tip to the IC pin in question, the LP-1 will give an instant picture of circuit conditions. Two level detector LED's (HI for logic "1" and LO for logic "0") and a blinking PULSE detector LED display the signal activity. One-shot, low-repetition-rate, narrow pulses are stretched to ⅓ second. A PULSE/MEMORY switch allows one shot events positive or negative transitions to be stored indefinitely. High frequency signals cause the PULSE LED to blink on and off at a 3 Hz rate. When the high frequency signals are unsymmetrical, there is an additional indication. Duty cycles less than 30% activate the LO LED; duty cycles above 70% activate the HI LED. **Input Impedance:** 100,000 ohms. **Threshold:** DTL/TTL, 2.25 V ±0.15 V equals "Logic 1", 0.80 V ±0.01 V equals "Logic 0"; HTL/CMOS, 70% of Vcc equals "Logic 1", 30% of Vcc equals "Logic 0". **Minimum Detectable Pulse Width:** 50 nanoseconds. **Input Frequency:** Up to 10 MHz. **Input Overload Protection:** ±50 V continuous; 117 VAC for less than 15 seconds. **Size:** 5.8" l. x 1.0" w. x 0.7" d. **Weight:** 3 ozs. **Power Required:** 30 mA at 5 VDC; 40 mA at 15 VDC; 36 V max. with polarity reversal protection.
CSC Model LP-1 Logic Probe—Complete. List Price ... $44.95

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2N2219A	NPN General Purpose	TO-5	.23	.17	.16	.15
2N2369A	NPN High Speed Switch	TO-92	.23	.165	.155	.135
2N2905A	PNP Small Sig. General Purpose	TO-5	.22	.20	.18	.17
2N2907A	PNP General Purpose	TO-18	.21	.175	.165	.155
2N3392	NPN Small Signal G.P.	TO-92	.19	.15	.14	.13
2N3414	NPN Gen. Purpose Switch	TO-92	.20	.19	.185	.18
2N3563	NPN Small Signal HF	TO-92	.24	.165	.14	.13
2N3565	NPN Low Level High Gain	TO-92	.24	.165	.14	.13
2N3638	PNP Sm. Sig. GP Amp.	TO-106	.24	.165	.14	.13
2N3640	PNP Hi Speed Sat. Switch	TO-92	.24	.165	.14	.13
2N3646	NPN Hi Speed Sat. Switch	TO-92	.24	.165	.14	.13
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2N3906	PNP Sm Sig. GP Amp.	TO-92	.23	.15	.14	.13
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2N4125	PNP Sm. Sig. GP Amp.	TO-92	.23	.15	.14	.13
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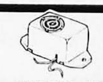
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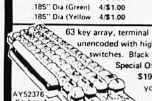


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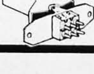
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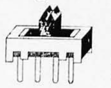


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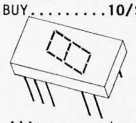
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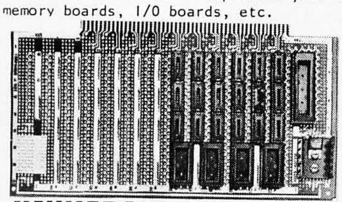
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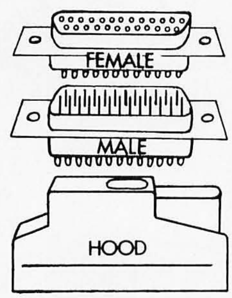
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* All TTL support ICs are latest Low Power Schottky types
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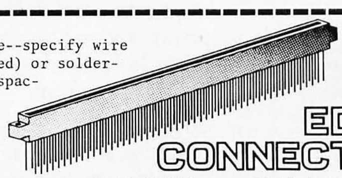
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8K X 8 BOARD $269.95 **2K X 8 BOARD $135.00**

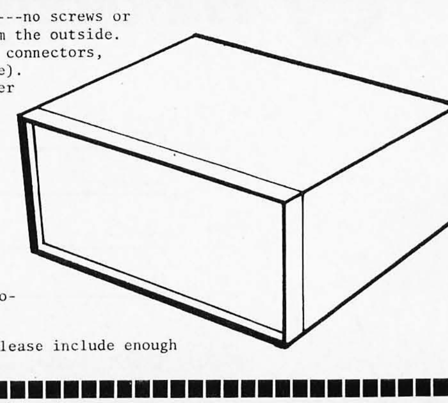
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74LS08	.29	74LS83	1.75	74LS163	2.25
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74LS32	.39	74LS109	.59	74LS195	1.89
74LS40	.39	74LS112	.59	74LS257	1.75
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MOS CLOCK CIRCUITS

FTK0400	Digital Clock/Calendar Circuit (FCM7001)	7.00
FTK0401	Digital Clock/Calendar with BCD Outputs (FCM7002)	7.00
FTK0402	Direct Drive Digital Clock Circuit with AC Output (FCM3817A)	5.00
FTK0403	Direct Drive Digital Clock Circuit with DC Output (FCM3817D)	5.00
FTK0405	Direct Drive Digital Clock/Calendar Circuit (FCM7015)	6.00

KITS

FTK0106	Automobile Clock Kit	40.00

DISCRETE LEDS

.125" dia.			.90" dia.		
XC209	Red	10/$1	XC111	Red	10/$1
XC209	Green	4/$1	XC111	Green	4/$1
XC209	Orange	4/$1	XC111	Yellow	4/$1
			XC111	Orange	4/$1

.200" dia			.185" dia.			.200" dia.			.085" dia.
XC22	Red	10/$1	XC526	Red	10/$1	XC556	Red	10/$1	MV50
XC22	Green	4/$1	XC526	Green	4/$1	XC556	Green	4/$1	.085" dia. Micro
XC22	Yellow	4/$1	XC526	Yellow	4/$1	XC556	Yellow	4/$1	red LED
XC22	Orange	4/$1	XC526	Orange	4/$1	XC556	Orange	4/$1	6/$1
SSL-22	RT	4/$1	XC526	Clear	4/$1	XC556	Clear	7/$1	

DISPLAY LEDS

DL707 DL33B

TYPE	POLARITY	HT		TYPE	POLARITY	HT	
MAN 1	Common Anode	.270	2.95	MAN 3620	Common Anode-orange	.300	1.75
MAN 2	5 x 7 Dot Matrix	.300	4.95	MAN 3640	Common Cathode-orange	.300	1.75
MAN 3	Common Cathode	.125	.39	MAN 4710	Common Anode-Red	.400	1.95
MAN 4	Common Cathode	.187	1.95	DL701	Common Anode-red ±	.300	.99
MAN 7	Common Anode	.300	1.25	DL704	Common Cathode	.300	.99
MAN 7G	Common Anode-green	.300	1.95	DL707	Common Anode	.300	.99
MAN 7Y	Common Anode-yellow	.300	1.95	DL 728	Common Cathode	.500	1.95
MAN 52	Common Anode-green	.300	1.75	DL 747	Common Anode	.600	2.25
MAN 64	Common Anode-red	.400	1.75	DL 750	Common Cathode	.600	2.49
MAN 72	Common Anode	.300	1.25	DL 33B	Common Cathode	.110	.50
MAN 74	Common Cathode	.300	1.50	FND70	Common Cathode	.250	.75
MAN 82	Common Anode-yellow	.300	1.75	FND503	Common Cathode	.500	1.00
MAN 84	Common Cathode-yellow	.300	1.75	FND507	Common Anode	.500	1.00

IC SOLDERTAIL — LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin	$.17	.16	.15	24 pin	$.38	.37	.36
14 pin	.20	.19	.18	28 pin	.45	.44	.43
16 pin	.22	.21	.20	36 pin	.60	.59	.58
18 pin	.29	.28	.27	40 pin	.63	.62	.61
22 pin	.37	.36	.35				

SOLDERTAIL STANDARD (TIN)

14 pin	$.27	.25	.24	28 pin	$.99	.90	.81
16 pin	.30	.27	.25	36 pin	1.39	1.26	1.15
18 pin	.35	.32	.30	40 pin	1.59	1.45	1.30
24 pin	.49	.45	.42				

SOLDERTAIL STANDARD (GOLD)

8 pin	$.30	.27	.24	24 pin	$.70	.63	.57
14 pin	.35	.32	.29	28 pin	1.10	1.00	.90
16 pin	.38	.35	.32	36 pin	1.75	1.40	1.26
18 pin	.52	.47	.43	40 pin	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

10 pin	$.45	.41	.37	24 pin	$1.05	.95	.85
14 pin	.39	.38	.37	28 pin	1.40	1.25	1.10
16 pin	.43	.42	.41	36 pin	1.59	1.45	1.30
18 pin	.75	.68	.62	40 pin	1.75	1.55	1.40

PUSH BUTTON SWITCH

PB-123 $1.75
Maintained Action Switch
PB-126 $1.75
Momentary Action Switch
SPDT

MINATURE TOGGLE SWITCH

JMT-221	DPDT	on/off/on	$1.95
JMT-223	DPDT	on/none/on	$1.75
JMT-121	SPDT	on/off/on	$1.50
JMT-123	SPDT	on/none/on	$1.25



CLIPLITE NEW LED MOUNTING SYSTEM — to be used with XC556 LEDS — **SPECIFY COLORS** — RED — GREEN — AMBER — YELLOW ***4/$1.00***

50 PCS. RESISTOR ASSORTMENTS $1.75 PER ASST.

ASST. 1	5 ea.	10 OHM / 27 OHM	12 OHM / 33 OHM	15 OHM / 39 OHM	18 OHM / 47 OHM	22 OHM / 56 OHM	1/4 WATT 5% = 50 PCS.
ASST. 2	5 ea.	68 OHM / 180 OHM	82 OHM / 220 OHM	100 OHM / 270 OHM	120 OHM / 330 OHM	150 OHM / 390 OHM	1/4 WATT 5% = 50 PCS.
ASST. 3	5 ea.	470 OHM / 1.2K	560 OHM / 1.5K	680 OHM / 1.8K	820 OHM / 2.2K	1K / 2.7K	1/4 WATT 5% = 50 PCS.
ASST. 4	5 ea.	3.3K / 8.2K	3.9K / 10K	4.7K / 12K	5.6K / 15K	6.8K / 18K	1/4 WATT 5% = 50 PCS.
ASST. 5	5 ea.	22K / 56K	27K / 68K	33K / 82K	39K / 100K	47K / 120K	1/4 WATT 5% = 50 PCS.
ASST. 6	5 ea.	150K / 390K	180K / 470K	220K / 560K	270K / 680K	330K / 820K	1/4 WATT 5% = 50 PCS.
ASST. 7	5 ea.	1M / 2.7M	1.2M / 3.3M	1.5M / 3.9M	1.8M / 4.7M	2.2M / 5.6M	1/4 WATT 5% = 50 PCS.

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) **$10.95 ea.**

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- Wraps 30 AWG Wire onto Standard DIP Sockets (.025 inch)
- Complete with built-in bit and sleeve

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WIRE-WRAP KIT — WK-2-W

WRAP • STRIP • UNWRAP



- Tool for 30 AWG Wire
- Roll of 50 ft. White 30 AWG Wire
- 50 pcs. each 1", 2", 3" & 4" lengths — pre-stripped white wire

$11.95

WIRE WRAP TOOL WSU-30
WRAP • STRIP • UNWRAP - $5.95

WIRE WRAP WIRE — 30 AWG

25 ft. min. $1.25 50 ft. $1.95 100 ft. $2.95 1000 ft. $15.00
SPECIFY COLOR — White - Yellow - Red - Green - Blue - Black

THUMBWHEEL SWITCHES

THUMBWHEEL SWITCH ONLY

Part No.	Description	Price
SF 12	Single Pole 10 Position	$2.50
SR 12	Decimal	3.00
SF 21	10 Position BCD only	2.50
SR 21		3.00

Ordering: Order desired switch or switches and add necessary accessories for your particular application.

SF — Front Mount SR — Rear Mount

SERIES SF Front Mount Assembly

SERIES SR Rear Mount Assembly

ACCESSORIES

Part No.	Description	Price
SF EP	End Plate (Pair)	.50
SF DP	Divider Plate (each)	.40
SF BB	Blank Body (each)	.40
SF HB	Half Body (each)	.40

ACCESSORIES

Part No.	Description	Price
SR EP	End Plates (pair)	$ .50
SR DP	Divider Plate (each)	.40
SR BB	Blank Body (each)	.40
SR HB	Half Body (each)	.40

DIP SWITCH

These switches feature seven SPST slide switches in a molded dip. They are ideally suited for microprocessor applications.

$1.95

ZENERS — DIODES — RECTIFIERS

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
1N746	3.3	400mm	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N751A	5.1	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N3600	50	200m	6/1.00
1N754	6.8	400m	4/1.00	1N4148	75	10m	15/1.00
1N959	8.2	400m	8/1.00	1N4154	35	10m	12/1.00
1N965B	15	400m	4/1.00	1N4305	75	25m	20/1.00
1N5232	5.6	500m	.28	1N4734	5.6	1w	.28
1N5234	6.2	500m	.28	1N4735	6.2	1w	.28
1N5235	6.8	500m	.28	1N4736	6.8	1w	.28
1N5236	7.5	500m	.28	1N4738	8.2	1w	.28
1N456	25	40m	6/1.00	1N4742	12	1w	.28
1N458	150	7m	6/1.00	1N4744	15	1w	.28
1N485A	180	10m	6/1.00	1N1183	50 PIV	35 AMP	1.60
1N4001	50 PIV	1 AMP	12/1.00	1N1184	100 PIV	35 AMP	1.70
1N4002	100 PIV	1 AMP	12/1.00	1N1185	150 PIV	35 AMP	1.50
1N4003	200 PIV	1 AMP	12/1.00	1N1186	200 PIV	35 AMP	1.80
1N4004	400 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR	$1.95
C38M	35A @ 200V	SCR	1.95
2N2328	1.6A @ 200V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC.	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC.	1.95

TRANSISTORS

MPS A05	5/$1.00			PN4249	4/$1.00
MPS A06	5/$1.00			PN4250	4/$1.00
2N2219A	3/$1.00	PN3567	3/$1.00	2N4400	4/$1.00
2N2221	4/$1.00	PN3568	4/$1.00	2N4401	4/$1.00
2N2222A	5/$1.00	PN3569	4/$1.00	2N4402	4/$1.00
2N2369	5/$1.00	2N3704	5/$1.00	2N4403	4/$1.00
2N2369A	4/$1.00	2N3705	5/$1.00	2N4409	5/$1.00
FN2415	5/$1.00	2N3706	5/$1.00	2N5086	4/$1.00
2N2484	4/$1.00	2N3707	5/$1.00	2N5087	4/$1.00
2N2906A	4/$1.00	2N3711	5/$1.00	2N5088	4/$1.00
2N2907A	5/$1.00	2N3724	$ .65	2N5089	4/$1.00
2N2925	5/$1.00	2N3725	$1.00	2N5129	5/$1.00
2N3053	2/$1.00	2N3903	5/$1.00	2N5138	5/$1.00
2N3055	$ .89	2N3904	4/$1.00	2N5139	5/$1.00
MJE3055	$1.00	2N3905	4/$1.00	2N5209	5/$1.00
MJE2955	$1.25	2N3906	4/$1.00	2N5951	5/$1.00
2N3392	5/$1.00	2N4013	3/$1.00	C106B1SCR	2/$1.00
2N3398	5/$1.00	2N4014	3/$1.00	2N5432	$2.00
		2N4123	10/$1.00		

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-49	50-100		1-9	10-49	50-100
10 pf	.05	.04	.03	.001µF	.05	.04	.035
22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075
100 VOLT MYLAR FILM CAPACITORS							
.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22
+20% DIPPED TANTALUMS (SOLID) CAPACITORS							
.1/35V	.28	.23	.17	1.5/35V	.30	.26	.21
.15/35V	.28	.23	.17	2.2/25V	.31	.27	.22
.22/35V	.28	.23	.17	3.3/25V	.31	.27	.22
.33/35V	.28	.23	.17	4.7/25V	.32	.28	.23
.47/35V	.28	.23	.17	6.8/25V	.36	.31	.25
.68/35V	.28	.23	.17	10/25V	.40	.35	.29
1.0/35V	.28	.23	.17	15/25V	.63	.50	.40
MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS							
Axial Lead				**Radial Lead**			
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.15	.13	.10	1.0/16V	.15	.13	.10
4.7/25V	.16	.14	.12	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

F8 EVALUATION BOARD KIT WITH EXPANSION CAPABILITIES

A fantastic bargain for only **$99.00** with the following features:

- 20 ma of RS 232 interface
- 64K addressing range
- Program control timers
- 1K off on board static memory
- Built in clock generator
- 64 Byte register
- Built-in priority interrupts
- Documentation

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This power suppy kit features a high frequency torroid transformer with switching transistors in order to save space and weight. 115V 60 cycle primary. The outputs with local regulators are +5V at 10A, −5V at 1A, ±12V at 1A.

$79.00

UNIVERSAL 4K × 8 MEMORY BOARD KIT

$74.50

This memoryboard kit can be used with most microcomputers. Some of the outstanding features are: 32-2102-1 static RAM's, 16 address lines, 8 data lines in, 8 data lines out, all buffered. On board decoding for any 4 of 64 pages.

4K F8 Basic $25.00

2522 STATIC SHIFT RE6 . . . . . $2.75
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2102-1 1024 BT RAM $1.80
5280-4K DYNAMIC RAM $10.50
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MM5203 UV PROM. $10.50
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100, 500, 2K, 10K, 100K, 200K
$.75 each . . . . 3/$2.00

MULTI-TURN TRIM POTS Similar to Bourns 3010 style 3/16"x5/8"x1-1/4"; 50, 100, 1K, 10K, 50K ohms
$1.50 ea. . . . . 3/$4.00

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TO-18, 200V 1A. . . . . $ 1.75

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2N3585 NPN Si TO-66 . . . . $ .95
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2N4908 PNP Si TO-3 . . . . $ 1.00
2N6056 NPN Si TO-3 Darlington . $ 1.70
2N5086 PNP Si TO-92 . . . . 4/$ 1.00
2N4898 PNP TO-66 . . . . $ .60
2N404 PNP GE TO-5 . . . . . . 5/$ 1.00
2N3919 NPN Si TO-3 RF . . . . . . $ 1.50
MPSA 13 NPN Si TO-92 . . . . . 3/$ 1.00
2N3767 NPN Si TO-66 . . . . $ .70
2N2222 NPN Si TO-18 . . . . 5/$ 1.00
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2N3904 NPN Si TO-92 . . . . 5/$ 1.00
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4006–1.20	4019– .22	4050– .40
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4010– .42	4028– .88	4076– .70
4011– .22	4029–1.10	4081– .22
4012– .22	4030– .22	4520–1.15
4013– .40		

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FND 500-.5" C.C. $1.75
HP 7740-.3" C.C. $1.40
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NS 33-3 dig. array $1.35
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This board is a 1/16" single sided paper epoxy board, 4½"x6½" DRILLED and ETCHED which will hold up to 21 single 14 pin IC's or 8, 16, or LSI DIP IC's with busses for power supply connector. $4.00

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MOLEX PINS . . . . 100/$1.00
1000/$7.50
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10 WATT ZENERS 3.9, 4.7, 5.6, 8.2, 12, 15, 18, 22, 100, 150 or 200V . . . ea. $ .60
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Silicon Power Rectifiers

PRV	1A	3A	12A	50A	125A
100	.06	.14	.30	.80	3.70
200	.07	.20	.35	1.15	4.25
400	.09	.25	.50	1.40	6.50
600	.11	.30	.70	1.80	8.50
800	.15	.35	.90	2.30	10.50
1000	.20	.45	1.10	2.75	12.50

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2¼" diameter
.4V at 500 ma. . . . $5.00 ea., 6/$27.50

REGULATED MODULAR POWER SUPPLIES

+– 15 VDC AT 100ma 115VAC INPUT $27.95
5VDC AT 1A, 115VAC INPUT . . . $24.95
12 VDC AT .5 AMP $24.95
IN 4148 (IN914) . . . . 15/$1.00

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.22UF 35V 5/$1.00	4.7UF 35V 4/$1.00
.47UF 35V 5/$1.00	6.8UF 35V 3/$1.00
.68UF 35V 5/$1.00	22UF 35V $ .40
1UF 35V 5/$1.00	33UF 35V $ .40
2.2UF 20V 5/$1.00	30UF 6V 5/$1.00
3.3UF 35V 4/$1.00	100UF 35V $ .50
	150UF 15V $ .50

M7001 ALARM CLOCK CHIP. . . . $6.00

NATIONAL MOS DEVICES

MM1402– 1.75	MM5057– 2.25
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MM5016– 2.50	MM5555– 4.75
MM5017– 2.70	MM5556– 4.75
MM5055– 2.25	MM5210– 1.95
MM5056– 2.25	MM5260– 1.75

30 WIRE WRAP WIRE SINGLE STRAND 100 FT. $1.40

TTL IC SERIES

7400– .15	7442– .52	74125– .40
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7403– .15	7447– .70	74153– .65
7404– .20	7448– .70	74154–1.10
7405– .20	7450– .20	74155– .70
7406– .25	7472– .33	74157– .70
7407– .25	7473– .35	74161– .85
7408– .25	7474– .35	74164– .95
7409– .21	7475– .49	74165–1.05
7410– .15	7476– .35	74173–1.40
7411– .20	7480– .35	74174– .95
7412– .20	7483– .70	74175– .92
7413– .45	7485– .88	74177– .79
7414– .70	7486– .30	74180 .70
7416– .25	7489–1.85	74181–2.10
7417– .25	7490– .45	74190–1.20
7420– .20	7491– .70	74191–1.20
7425– .28	7492– .50	74192– .85
7426– .25	7493– .45	74193– .85
7427– .30	7494– .70	74194– .85
7430– .20	7495– .70	74195– .75
7432– .25	7496– .70	74196– .88
7437– .25	74107– .32	75324–1.75
7438– .25	74121– .38	75491– .65
7440– .16	74123– .65	75492– .65
7441– .85		

MINIATURE DIP SWITCHES

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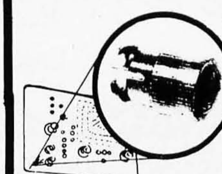
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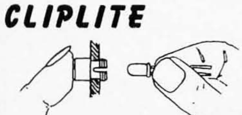
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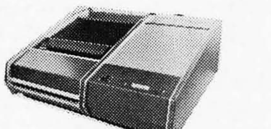
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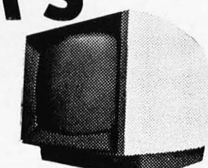


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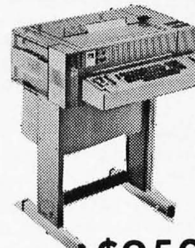
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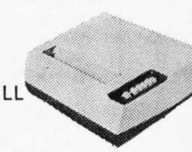
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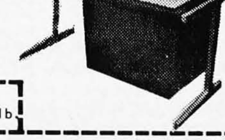


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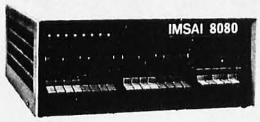


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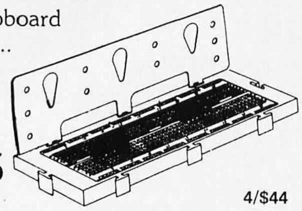


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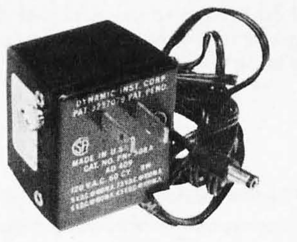
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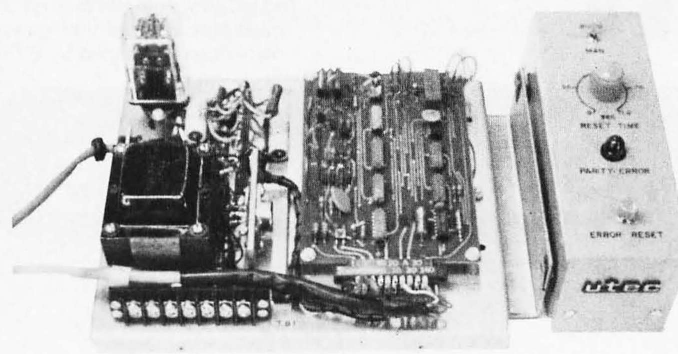
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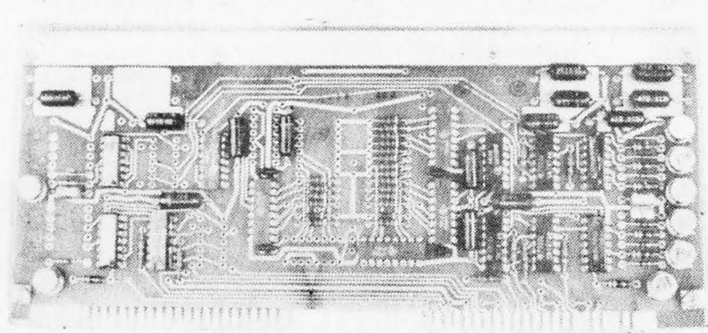
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